Public University of Navarra
Electrical, Electronic and Communications Engineering Department

POWER-EFFICIENT CMOS CIRCUITS FOR ENERGY HARVESTING SUPPLIED IoT SYSTEMS

PhD. Dissertation prepared to obtain the Doctor degree with the International Doctorate Mention

By

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A MI FAMILIA Y AMIGOS

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ABSTRACT

In this thesis, innovative low voltage and low power techniques have been applied to implement novel analog circuits (mainly amplifiers). These circuits are suitable for energy autonomous devices such as those required in many Internet of Things (IoT) scenarios. The structure of the thesis is as follows: basic techniques for low voltage low power operation are proposed, at both cell and device level, followed by several novel basic building blocks using them and finally the achievement of new designs at subsystem level.

At circuit level, different power efficient amplifiers are proposed in this work. They are obtained by combining different low voltage techniques. The main ones are the use of Quasi-Floating Gate (QFG) transistors some adaptive biasing techniques (the Flipped Voltage Follower, or FVF, and the Local Common-Mode Feedback, or LCMFB, among others). These schemes can be applied to single-ended or to fully differential amplifiers, leading to different topologies. The proposed circuits are compared with other relevant publications, showing a very competitive performance.

At subsystem level, another low voltage technique, which is based in the use of floating voltage sources, is employed to design three blocks, two of them related to A/D conversion.

The proposed circuits have been fabricated using different CMOS technologies (130 nm, 180 nm and 0.5 μm) and the corresponding measurement results are provided and analyzed to validate their operation. In addition, theoretical analysis has been done to fully explore the potential of the resulting circuits and systems in the scenario of low-power low-voltage applications.

RESUMEN

En esta tesis, se han aplicado técnicas de baja tensión y bajo consumo para implementar nuevos circuitos analógicos (principalmente amplificadores). Estos circuitos están orientados a dispositivos energéticamente autónomos como los utilizados en muchos escenarios del Internet de las Cosas (IoT). La estructura de la tesis es la siguiente: se proponen técnicas básicas para operación en baja tensión y bajo consumo, tanto a nivel de celda como a nivel de dispositivo, seguido por varios bloques básicos novedosos que utilizan dichas técnicas y finalmente por la obtención de nuevos diseños a nivel de subsistema.

A nivel de celda, diferentes amplificadores energéticamente eficientes se proponen en este trabajo. Estos se obtienen combinando diferentes técnicas de baja tensión. Las principales son el uso de transistores de puerta cuasi-flotante (Quasi-Floating Gate o QFG) y algunas técnicas de polarización adaptativa, entre las que destacan el seguidor de tensión plegado (en inglés, Flipped Voltage Follower o FVF) y la realimentación local de modo común (Local Common-Mode Feedback o LCMFB). Estas técnicas pueden aplicarse tanto a amplificadores diferenciales como no diferenciales, creando así diferentes topologías. Los circuitos propuestos se comparan con otras publicaciones relevantes, mostrando un funcionamiento muy competitivo.

A nivel de subsistema, otra técnica de baja tensión, basada en el uso de fuentes de tensión flotantes, se emplea para diseñar tres bloques, dos de los cuales están relacionados con la conversión analógico-digital (A/D).

Los circuitos propuestos han sido fabricados usando diferentes tecnologías CMOS (130 nm, 180 nm y 0.5 μm) y los correspondientes resultados de las medidas son presentados y analizados para validar su funcionamiento. Además, se han realizado análisis teóricos para explorar el potencial de los circuitos y subsistemas resultantes en aplicaciones de bajo consumo y baja tensió

LIST OF ACRONYMS

Acronym	Significance
ADC	Analog to Digital Converter
AC	Alternating Current
BW	Bandwidth
CA	Current Amplifier
CE	Current Efficiency
CF	Current Follower
CM	*1)* Common Mode *2)* Current Mirror
CMFB	Common Mode Feedback
CMIR	Common Mode Input Range
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
CMS	Common-Mode Sensor
DAC	Digital to Analog Converter
DC	Direct Current
DDA	Difference Differential Amplifier
DM	Differential Mode
EA	Error Amplifier
FC	Folded Cascode
FDA	Fully Differential Amplifier
FG	Floating-Gate
FGMOS	Floating-Gate Metal-Oxide-Semiconductor
FGT	Floating-Gate Transistor
FVF	Flipped Voltage Follower
FoM	Figure of Merit
GBW	Gain-Bandwidth Product

IC	Integrated Circuit
LCMFB	Local Common-Mode Feedback
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
NMOS	N-Channel Metal-Oxide-Semiconductor
opamp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PM	Phase Margin
PMOS	P-Channel Metal-Oxide-Semiconductor
PSRR+	Positive Power-Supply Rejection Ratio
PSRR-	Negative Power-Supply Rejection Ratio
QFG	Quasi-Floating-Gate
QFGMOS	Quasi-Floating-Gate Metal-Oxide-Semiconductor
QFGT	Quasi-Floating-Gate Transistor
RFC	Recycling Folded Cascode
SC	Switched Capacitor
SR	Slew Rate
THD	Total Harmonic Distortion
VLSI	Very-Large-Scale Integration

PARAMETER GLOSSARY

Parameter	Significance
C_{ds}	Drain-Source capacitance
C_{gd}	Gate-Drain capacitance
C_{gs}	Gate-Source capacitance
C_L	Load capacitor
C_{ox}	Gate Oxide capacitance per unit area
f_d	Dominant pole frequency
f_{nd}	Non-dominant pole frequency
g_m	MOS transistor transconductance defined as $\partial I_D/\partial V_{GS}$
G_m	Total transconductance of an OTA
I_B	Bias current
I_{CM}	Common-Mode current
I_{Di}	Drain current thought transistor M_i
K	*1)* Current scaling factor
	2) Mos transistor transconductance coefficient
K_B	Boltzmann constant ($1.38 \cdot 10^{-23}$ J / K)
L	Channel length of a MOS transistor
q	Electron charge
Q_0	Initial electric charge
R_{out}	Output resistance of an OTA
r_o	Small-signal equivalent drain-source resistance of a MOS transistor
T	Absolute temperature
t_{ox}	Oxide under the gate thickness
V_{CM}	Common-Mode voltage
V_{CMref}	Reference Common-Mode voltage

PARAMETER GLOSSARY

V_{CMctrl}	Common-Mode control voltage
V_{CN}	Bias voltage in a NMOS cascode transistor
V_{CP}	Bias voltage in a PMOS cascode transistor
V_{DD}	Positive supply voltage
V_{DDP}	Positive voltage slightly smaller than V_{DD}
V_{SD}, V_{DS}	Source-drain/Drain-source voltage of a MOS transistor
V_{SG}, V_{GS}	Source-gate/Gate-source voltage of a MOS transistor
V_{SS}	Negative supply voltage
V_{TH}	Threshold voltage of a MOS transistor
W	Channel width of a MOS transistor
μ_n	Electron mobility parameter

Chapter 1

INTRODUCTION

The main purpose of this introductory chapter is to present the framework of this thesis. In first place, the motivations of this work are discussed in Section 1.1. Afterwards, Section 1.2 targets the energy harvesting systems, emphasizing the requirements of low-voltage low-power operation. Section 1.3 is focused on presenting the objectives, and finally, the structure of the thesis is provided in Section 1.4.

1.1 Motivation

In the last few years, there has been a proliferation in the number of devices that are connected to the Internet. These gadgets can provide information about the environment where they are placed, by sensing certain parameters and making them “smart”. Thus, the concept of Internet of Things was created.

Internet of Things (IoT) refers to the interconnection of everyday objects thanks to the use of integrated electronics, allowing them to share data obtained by sensors. This information is processed to take advantage of it, and then it can be sent to a remotely located user.

Nowadays, most of the connected objects are smartphones, but recently other types of devices are used, such as home appliances or wearables. As Figure 1.1 [1] shows, it is expected that 21.5 billion devices will be interconnected by 2025 (without including smartphones, tablets, laptops and

fixed line phones). But not only domestic gadgets are likely to be part of the Internet of Things, but they can also be applied to other fields, such as industrial, military, medical, environmental or automotive.

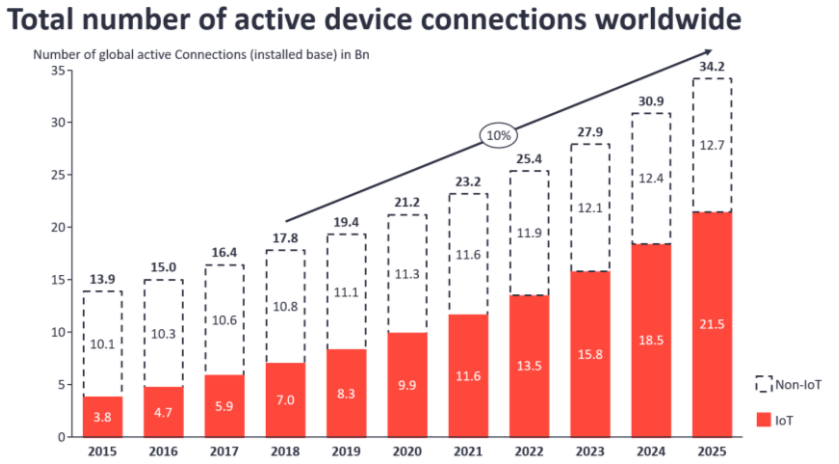

Figure 1.1: Expected growth of Internet of Things [1]

1.2 Energy harvesting in IoT

Energy is a critical issue in IoT. Apart from devices, also wireless networks are involved in the Internet of Things. Edge computing nodes must work in low power operation in order to be autonomous for a long period of time. Two approaches can be followed to supply these devices: the use of small batteries alone, or the employment of energy harvesting techniques able to recharge and therefore to increase the shelf life of such batteries, even avoiding the use of batteries in some cases. There are scenarios where the frequent replacement of batteries is inadequate (for example, in large networks) or not viable (e.g. sensor nodes embedded in the structure of a building). Some of them are:

- *Body Area Networks.* Biomedical sensor nodes are often placed inside the body, and an invasive surgery would be required to replace the batteries. The same situation happens with other biomedical devices, like pacemakers and implantable defibrillators. Furthermore, in some cases, the size of the device is a limiting factor (e.g. sensors circulating through the gastrointestinal tract), making the use of batteries unfeasible.

- *Environmental monitoring*. As it was said before, IoT also serves to monitor vast ecosystems, such as cities (to control pollution levels, to achieve energy efficiency, etc.), forests (to prevent fires), volcanos (to monitor volcanic and seismic activity) and crops (to control humidity, presence of plagues, etc.). The number and location of sensor nodes hinder the replacement of the batteries, thus causing the cost increase.
- *Industrial plants*. WSNs are also employed in harsh industrial environments for process monitoring and control. In these cases, battery replacement is also difficult. Furthermore, the battery lifetime is reduced when temperature is high, due to the acceleration of the self-discharge process.

An efficient alternative for these scenarios is the use of energy harvesting techniques. Thanks to this approach, energy is acquired from the environment and stored in a secondary battery or a supercapacitor in order to provide a stable power supply or to provide high peak currents when needed, e.g. during data transmission. Energy can be obtained from different sources, like wind, sound, light, movement or electromagnetic waves. This energy acquisition process is often referred to as energy scavenging or energy harvesting [1]. Although it seems that these terms are equivalent, there is a subtle different between them. In energy harvesting, the acquisition of energy is obtained from well-defined and continuous sources, whereas in energy scavenging, acquisition is made in environments with little knowledge and irregular availability of energy sources.

A typical wireless microsensor mote of a WSN is shown in Figure 1.2. The signal acquired by the sensor is processed by an analog front-end and converted to the digital domain by an Analog to Digital Converter (ADC). Afterwards, the signal is processed, stored in memory and sent by the transceiver unit. The power unit is responsible for extracting power from the power source and conditioning it adequately to power all the modules of the system.

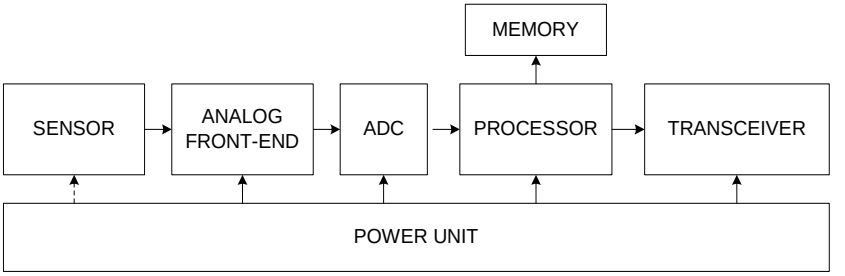

Figure 1.2: Conceptual scheme of a typical wireless mote

Figure 1.3 presents a typical energy harvesting system that can be used as power unit in Figure 1.2. An energy harvesting transducer captures the ambient energy, obtaining a DC or AC voltage, depending on the type of source. This energy is stored after being transformed by the DC/DC or AC/DC converter respectively. As mentioned, the storage element can be a supercapacitor or a secondary battery. At the end, a DC/DC converter regulates the voltage, in order to provide a stable voltage to the target circuit.

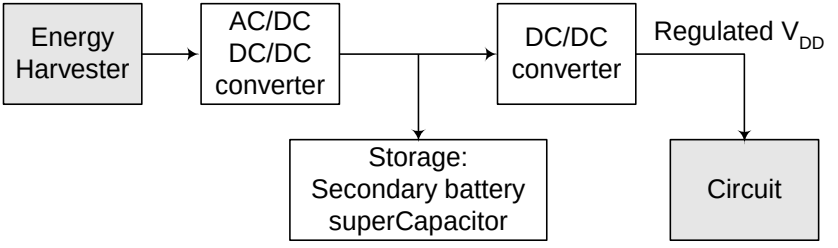

Figure 1.3: Typical energy harvesting microsystem

Different approaches are followed to design the converters before and after the storage device, as the objective of the first converter is to deliver optimally a charging current to the storage element and the aim of the second one is to regulate the output voltage.

Power density obtained depends on the type of source and the size of the energy harvesting transducer. Photovoltaic energy is usually the most reliable and efficient ambient energy source in outdoors, providing around 10 mW/cm^2. However, this type of energy is not suitable in some applications, such as wearables that also work in indoor environments.

Here is a list of different ambient energy sources, with a brief description. Note that features of renewable energy sources available in outdoor scenarios are completely different from those found in indoor spaces. In

addition, different types of indoor scenarios, such as domestic, commercial, industrial and medical, also show different conditions. Generally, ambient energy obtained inside buildings (factory, hospital, office, home…) are generated by artificial means as opposed to outdoor sources.

- *Solar energy*. In outdoor environments, it is the most successful and efficient mean of achieving energy autonomy. Solar cells can be placed in different locations, such as vineyards, parks, streets, etc., producing continuous high power density during daytime. However, indoor light harvesting is much less effective. Intense illumination is rare and highly localized inside a building, usually limited to the surroundings of windows. Hence, the most common places where light is accessible are around a light bulb or in the environment, being of a weak and scattered nature.

- *Wind.* Kinetic energy of moving air and other fluids can also be employed for harvesting energy. There are different generators, such as wind turbines [2], windbelt [3] or flapping piezoelectric [4]. Harvesting kinetic energy is less efficient in indoor scenarios, as it happened with solar energy.

- *Thermal.* Thermoelectric generators (TEG) are the most commonly used devices to harvest thermal energy from the ambient. They transform thermal gradients into electrical energy based on the Seebeck effect. TEG devices are based on a set of thermocouples, each one formed by a single pair of n- and p- type thermoelectric elements. Temperature differences between the two sides of the thermocouples result in heat flow, thus charge flow of dominant carriers from the high temperature end to the low temperature one, yielding to a voltage difference given by $V_G = N \cdot \alpha \cdot \Delta T$, where N is the number of thermocouples, α is the Seebeck coefficient of the thermoelectric materials, and ΔT is the temperature difference between the two sides.

- *Vibration.* Vibrations are a relevant source of energy in indoor applications, especially in industrial scenarios. They can be created by machines, human activity or vehicular traffic. There are different types of transducers. The most common ones are piezoelectric [5], inductive [6] or capacitive [7]. All these sources generate an AC signal; hence an AC/DC conversion is necessary before storing the harvested energy.

- *Radio-Frequency (RF).* Electromagnetic energy coming from radio waves can be collected using antennas [8]. The obtained AC voltage is rectified and then used. RFID tags use this type of energy. They are wirelessly powered by the reader device near the tag.

- *Radioactive sources* [9]. Despite providing the largest energy density (greater than 40000 W.h/cm^3 [1]), they are impractical, due to safety and environmental issues. As a result, atomic batteries have been proposed [10], which are devices that use energy from radioactive decay to generate electricity.

- *Acoustic energy* [11], [12]. Energy can also be collected from acoustic waves, using an acoustic transducer or resonator. In practice, this technique is only useful in very noisy environments, above 114 dB. It is estimated that acoustic energy harvesting can provide approximately 0.96 μW/cm^2, which is much lower than other energy harvesting methods previously described. In indoor applications this energy source is of little interest, unless in very noisy industrial plants.

Scheme shown in Figure 1.4 [13] classifies different energy sources, indicating the working principle in which they are based and the type of voltage they provide (AC or DC).

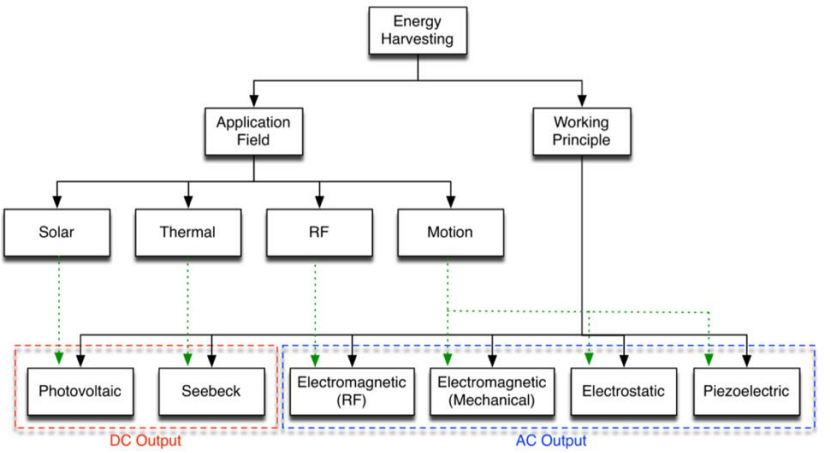

Figure 1.4. Classification of energy sources [13]

Table 1.1 [14] provides an estimation about power density obtained from different energy sources. From the information this table gives, the need for low voltage low power circuit design can be inferred.

Power source	Typical Power Density
Wind	28.5 mW/cm^2
Solar (outdoors)	15 mW/cm^2
Solar (indoors)	15 μW/cm^2
Thermal	15 μW/cm^2
Vibration (Electromagnetic transducer)	145 μW/cm^2
Vibration (Piezoelectric transducer)	330 μW/cm^2
Vibration (Electrostatic)	50 μW/cm^2
Ambient RF	12 nW/cm^2
Directed RF	50 mW/cm^2
Acoustic	96 μW/cm^2

Table 1.1. Power density of different harvesting power sources [14]

1.3 Objectives

IoT is not economically nor energetically feasible in several envisaged scenarios without a drastic reduction in the power consumption of IoT devices. In this sense, energy efficiency of these devices (and the use of energy harvesting in many cases) is a critical requirement in the deployment of IoT technologies and extensive research is required to achieve it. The design of microelectronic systems aimed to these scenarios is a notable engineering challenge as it requires pushing energy efficiency near the physical limit for the energy acquisition, storage and management systems and for the sensing, signal processing and communication systems.

The general purpose of this thesis is to design different analog and mixed-signal integrated circuits with improved performance aimed to these demanding IoT scenarios, which operate in low-voltage low-power conditions. In particular, the main objectives of this work are the following:

- To provide a brief summary of the state-of-the-art of several analog IC design techniques aimed not only to reduce the power consumption but also to improve the performance of different blocks.
- To apply these techniques in order to develop basic cells. Besides decreasing the supply voltages and power consumption, other parameters have been improved, such as Slew Rate (SR), DC gain (A_{DC}) or gain bandwidth product (GBW).
- To implement some subsystem level blocks, based on the amplifiers previously developed.

By fulfilling the above list of objectives, this thesis tries to contribute to low-voltage low-power amplifiers that can be used in Energy Harvesting supplied systems, considering their need to face the predicted growth of the number of devices connected to Internet of Things (IoT) systems.

1.4 Organization of the thesis

This thesis is divided in 7 chapters, being the first one this introductory chapter. The motivations of this work have been presented, along with an overview of Internet of Things systems. In addition, the main objectives of this thesis have been listed. The next paragraphs summarize the content of the other 6 chapters.

Chapter 2 shows different low voltage low power approaches employed in the following chapters. Not only device level techniques are explained, but also some circuit level topologies, aimed to design class AB amplifiers with improved performance.

An improved logic family is introduced in Chapter 3, able to operate below the threshold voltage. In addition, two possible applications are included.

In Chapter 4, several single-ended amplifier topologies are presented. They have been designed focusing on improving their performance while operating in low voltage conditions. Measurements are presented to validate the obtained results.

Different fully differential amplifiers are treated in Chapter 5. These blocks were also fabricated on a prototype chip. The measured results are presented.

Chapter 6 is focused on some subsystem-level circuits: a low voltage buffer, a Sample and Hold (S/H) and a Delta-Sigma modulator, working properly at very low supply voltages.

Finally, Chapter 7 sums up the general conclusions of this work. In addition, future research ideas are given.

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Chapter 2

LOW VOLTAGE AND LOW POWER TECHNIQUES

In order to extend the battery lifetime of an end node employed in IoT systems, two approaches can be followed: using a battery of higher capacity and/or decreasing the power consumption. The demand for portable and wearable devices of small size and weight is increasing, thus discarding the first option. As for the second option, decreasing quiescent power consumption is a good choice, because this component is present even when input signal is null. The quiescent power consumption is the product of the quiescent bias current (I_q) and the supply voltage (V_{DD}), thus in order to reduce it, it is necessary to lower any of these two parameters.

Concerning V_{DD}, the downscaling that CMOS technology is suffering in the last decades causes that the supply voltages have to adapt. They are getting really close to the threshold voltages of MOS transistors, which leads to degradation in terms of dynamic range. When supply voltage is reduced, the voltage headroom available is also decreased, and input transistors must be properly biased in order to operate well. In some cases, rail-to-rail operation must be enforced in order to get proper dynamic range. New approaches must be followed when designing circuits in order to process rail-to-rail signals.

On the other hand, when designing any circuit, quiescent current I_q can be decreased, e.g. reducing the number of branches, but not without limit, due to its impact on the performance of the block. Reducing I_q can cause degradation of the dynamic performance in some cases. In class A amplifiers, the maximum

output current is limited by the bias current I_B, thus limiting other parameters such as slew rate (SR = I_B/C_L) or settling time. In order to avoid this limitation, class AB amplifiers are widely used, because they can provide dynamic currents larger than the quiescent ones. Thanks to class AB stages, large Slew-Rate can be obtained for large signal operation with low I_B values, keeping low power consumption. There are different topologies to achieve class AB operation, but normally these options make the circuit more complex. In this thesis, several approaches in order to get class AB amplifiers are going to be presented, without scarifying the simplicity of the circuits.

In this chapter, some basic techniques are described that will be applied in following chapters. The main purposes of these circuits are:

- To decrease the power consumption without suffering a degradation in performance.
- To design class AB stages in order to avoid limitations in dynamic performance.
- To achieve rail-to-rail operation.
- To improve important parameters in amplifiers, such as GBW, DC gain, input equivalent noise, etc.

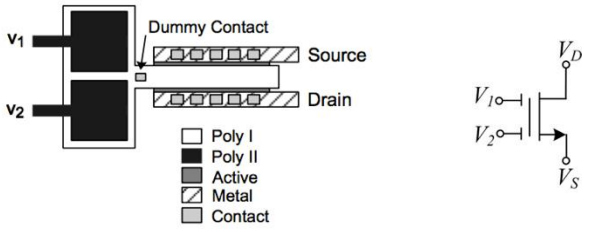
Section 2.1 contains some approaches that can be applied at device level, whereas in Section 2.2 some other topologies are explained, but this time at circuit level. To summarize, some conclusions are drawn.

2.1 Techniques at device level

As it has been said in the introduction of the chapter, different low-voltage low-power techniques can be considered at device level. Sections 2.1.1 and 2.1.2 are devoted to explain the Floating Gate (FG) and Quasi-Floating Gate (QFG) transistors, respectively. In Section 2.1.3, subthreshold operation is presented, while bulk driven topologies are shown in Section 2.1.4.

2.1.1 The Floating Gate MOS transistor (FGMOS)

The floating gate MOS transistors (hereinafter, named as FGMOS) was first reported in 1967 [1]. Since then, it has been widely used for analog design. A FGMOS transistor is characterized by having *n* input terminals capacitively coupled to the internal gate node. As there is no low resistance path to charge or discharge it, the internal gate node is floating in DC, hence its name. The layout and symbol of a two input FGMOS transistor is presented in Figure 2.1. As Figure 2.1(a) shows, the input capacitors C_k are formed by overlapping two poly layers.



(a) (b)

Figure 2.1. Two input FGMOS transistor (a) Layout (b) Symbol

Figure 2.2 represents the equivalent circuit of an *n*-input FGMOS transistor. Not only are the capacitors between the inputs and the floating gate terminal shown, but also the parasitic capacitances.

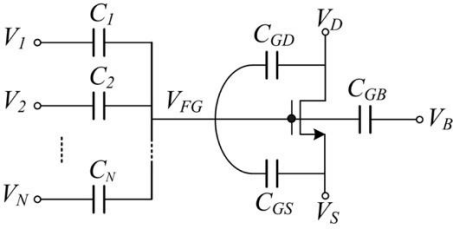


Figure 2.2: Equivalent circuit of an n input FGMOS transistor

As previously said, the floating gate of a FGMOS transistor is not able to charge or discharge itself. Thus, applying the charge conservation at the floating gate, the floating-gate transistor voltage will be:

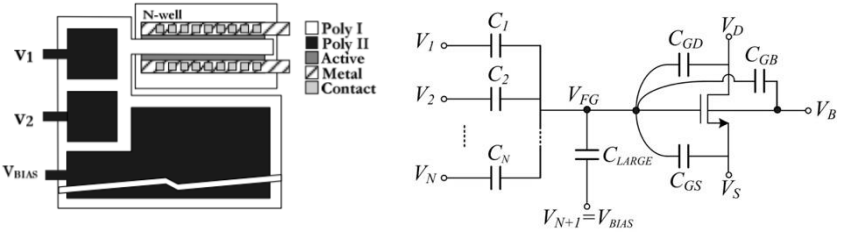
$$V_{FG} = \frac{1}{C_T}\left(\sum_{k=1}^{N} C_i V_i + C_{GS}V_s + C_{GD}V_D + C_{GB}V_B + Q_0\right) \qquad (2.1)$$

where $C_T = \sum_{k=1}^{N} C_i + C_{GS} + C_{GD} + C_{GB}$ and Q_0 is the initial charge trapped at the floating gate terminal during the fabrication process. This charge must be removed in order to avoid undesired DC offsets. Conventionally, UV radiation [2], [3], tunnel effect [4] or hot electron injection [5], [6] have been used to remove this trapped charge.

If Expression 2.1 is expanded and simplified, it can be observed that the voltage at the floating gate terminal is a weighted addition of the *n* input voltages, where each input voltage is scaled by the ratio between its coupling capacitance C_k and the total capacitance C_T, and some additional terms caused by parasitic capacitances.

$$V_{FG} = a_1 V_1 + \cdots + a_N V_N + \frac{C_{GS}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{C_{GB}}{C_T} V_B \; where \; a_k = \frac{C_k}{C_T} \quad (2.2)$$

If we want the FGMOS transistor to work properly for low supply voltage, the DC voltage at the floating gate must be close to one of the rails (V_{DD} in the case of a NMOS transistor or V_{SS} if it is a PMOS). To satisfy this condition, a new input (V_{N+1}) must be added connected to a DC level (V_{BIAS}), whose value is often V_{DD} or V_{SS} (depending on the type of transistor). The schematic of this configuration is shown in Figure 2.3.



(a) (b)

Figure 2.3. Multiple input FGMOS transistor (a) Layout (b) Equivalent circuit

Equation 2.3 characterizes the behavior of transistor in Figure 2.3. If we want V_{FG} to be close to one of the rails, it can be seen from expression 2.3 that C_{LARGE} must be much larger than the rest. As a result, there is a considerable increase of silicon area and a reduction of the Gain-Bandwidth (GBW) product if FGMOS transistors are used to form the input differential pair of an amplifier.

$$V_{FG} = \frac{C_{LARGE}}{C_T} V_{BIAS} + \frac{1}{C_T} \left(\sum_{i=1}^{N} C_i V_i + C_{GS} V_S + C_{GD} V_D + C_{GB} V_B + Q_0 \right) \quad (2.3)$$

Floating Gate transistors can be employed in order to achieve rail-to-rail input range, maximizing dynamic range at low supply voltages. Figure 2.4

shows the method, using a two-input n-type FGMOS transistor. The input voltage is applied to the floating gate transistor through a capacitor, C_2, while the other capacitor, C_1, is connected to the supply voltage. This way, one of the inputs biases the circuit and the other one processes the input signal. As a consequence, a capacitive divider is formed, scaling the input signal and shifting the DC level, thus permitting rail-to-rail input range despite the limited voltage range available at the gate of the FG transistor. This transformation can be seen in Figure 2.4. The resulting signal is a downscaled and shifted version of the input one.

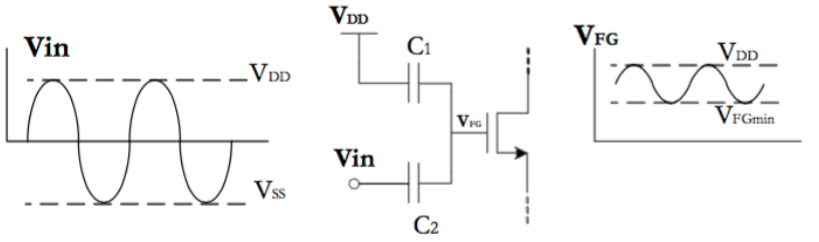


Figure 2.4. Rail-to-rail operation with FGMOS techniques

If zero initial charge is assumed and parasitic capacitances are neglected, the expression of the floating gate voltage can be obtained from Expression 2.1.

$$V_{FG} = \frac{C_1}{C_1+C_2} V_{DD} + \frac{C_2}{C_1+C_2} V_{in} \tag{2.4}$$

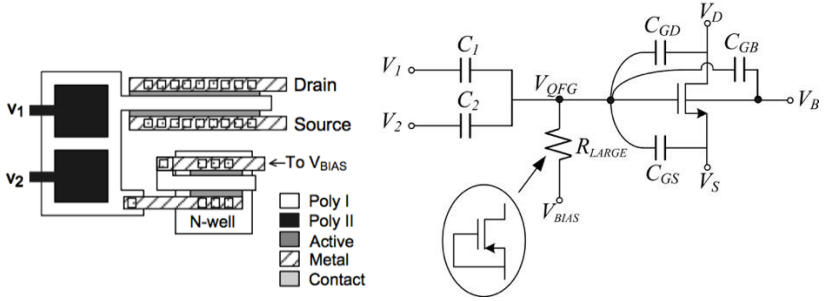
The input signal suffers an attenuation factor $a = C_2 / (C_1 + C_2)$ and its DC voltage is shifted by $V_{DC} = V_{DD}.C_1 / (C_1 + C_2)$. Proper values of capacitors C_1 and C_2 must be chosen, because when $V_{in} = V_{DD}$, V_{FG} is also V_{DD}, but when $V_{in} = V_{SS}$, V_{FG} depends on the ratio of these capacitors. Thus, in order to achieve rail-to-rail operation, the floating gate voltage must be high enough to properly bias the device.

If this technique is applied to a p-type FGMOS transistor, the process is similar except for the DC supply voltage, which must be replaced by V_{SS} to perform a down-shifting.

An improvement in linearity is obtained, as the input attenuation reduces the signal swing. Nonetheless, input-referred noise voltage is also increased by a factor 1/*a*.

2.1.2 The Quasi-Floating Gate MOS transistor (QFGMOS)

The quasi-floating gate MOS transistor (or QFGMOS from now on) was designed to solve these issues [7]. Instead of using a large capacitor to bias the gate of the transistor, a large resistor R_{large} is employed. The layout and equivalent circuit of a 2-input QFGMOS transistor are shown in Figure 2.5. Note that the large resistance R_{large} can be implemented by the leakage resistance of a reverse-biased pn junction of a MOS transistor connected in diode configuration operating in cutoff region [8]-[10]. The area of this MOS transistor can be minimal, thus saving area compared to Figure 2.3. The DC voltage at the gate of the QFGMOS transistor is set to V_{BIAS} independently of the different DC voltages of the input signals.



(a) (b)

Figure 2.5. Two-input QFGMOS transistor (a) Layout (b) Equivalent circuit

The quasi-floating gate AC voltage of an *n* input QFGMOS transistor follows the Expression 2.5. According to this equation, the AC input signals are scaled by the ratios between capacitances, in addition to some parasitic terms. Moreover, they experience a high-pass filtering with a cutoff frequency $f_c = 1/(2\pi R_{large} C_T)$, which can have very low values, even below 1 Hz.

$$V_{QFG} = \frac{sR_{large}}{1+sR_{large}C_T}\left(\sum_{i=1}^{N} C_i V_i + C_{GS}V_S + C_{GD}V_D + C_{GB}V_{bias}\right) \quad (2.5)$$

Note that the exact value of R_{large} is not relevant as long as it is large enough to achieve a cutoff frequency lower than the minimum input frequency.

QFGMOS transistors can contribute to obtain class AB operation very efficiently [11]. Figure 2.6(a) presents the basic class AB output stage with a floating battery.

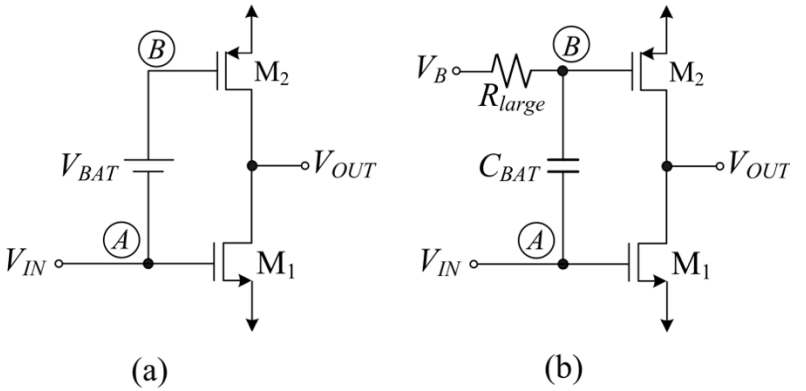


Figure 2.6. QFG class AB output stage (a) Floating battery implementation (b) QFGMOS implementation

Thanks to the floating battery, node *B* follows the voltage variations at node *A* shifted by a DC voltage V_{BAT}. In static conditions, current is determined by node *A* voltage plus a DC level corresponding to V_{BAT}. But in dynamic conditions, node *B* experiences the same changes as the input signal thanks to the transfer from node *A*, thus the output current can achieve values larger than the quiescent current. Diverse approaches have been followed to implement the DC level shifter, but they require extra quiescent power consumption, and they may increase supply voltage requirements. In addition, the quiescent current is often not accurately set and depends on process and temperature variations, and the parasitic capacitances added by this extra circuitry can limit bandwidth.

A simple way of implementing the floating battery is by using a QFGMOS transistor [12], as shown in Figure 2.6(b). When input signal is null, the output current is I_B, as the capacitor behaves as an open circuit in DC. However, under dynamic conditions, R_{large} and C_{BAT} form a high pass filter. Thus, node *A* transfers the input variation to node *B* with an attenuation factor of $\alpha = C_{BAT} / (C_{BAT} + C_B)$ and high-pass filtered with a cutoff frequency $f_c = 1/ (2\pi R_{large}\cdot(C_{BAT} + C_B))$, being C_B the capacitance at node B, that can be estimated as $C_B = C_{gs} + C_{gd} \approx C_{gs}$. As the value of R_{large} is in the order of GΩ, the value of the cutoff frequency is going to be very small, typically below 1 Hz, filtering out only the DC voltage component of the input signal.

The main benefit of this class AB stage is that the Slew-Rate experiences a considerable improvement in large-signal operation. Considering

C_L as the output capacitance load, the expression of the Slew Rate is $SR = I_{out}^{max}/C_L$, not limited by bias current I_B.

2.1.3 Sub-threshold operation: weak inversion

In the 70s, some pioneering works were published trying to model the weak inversion operation of a CMOS transistor [13]-[19]. At that time, minimum supply voltage requirements were not a problem. However, nowadays CMOS processes are downscaling their supply voltages, but not so fast their threshold voltages. Sub-threshold operation allows working with very low V_{GS} voltages, below the threshold voltage: Hence they are adequate for low voltage operation.

Two of the most important parameters in transistor design are the drain current and the transconductance gain. Equations 2.6 and 2.7 express these parameters for weak inversion, whereas 2.8 and 2.9 show the same parameters for strong inversion operation [19]-[24].

$$I_{D,wi} = 2n\beta U_T^2 e^{\left(-V_{T0}/nU_T\right)} e^{\left(V_{GS}/nU_T\right)} \tag{2.6}$$

$$g_{m,wi} = \frac{I_D}{nU_T} \tag{2.7}$$

$$I_{D,si} = \frac{\beta}{2}(V_{GS} - V_{TH})^2 \tag{2.8}$$

$$g_{m,si} = \sqrt{2\beta I_D} \tag{2.9}$$

where $\beta = (\mu_n C'_{ox} W)/L$, n is the slope factor, μ_n is the mobility of electrons near the surface, C'_{ox} is the gate capacitance, W and L are the transistor dimensions, V_{TH} is the threshold voltage and $U_T = kT/q$ is the thermal voltage.

If drain current expressions are compared, it can be seen that relationship between V_{GS} and I_D is exponential in the weak inversion model, whereas in the strong inversion model it is quadratic. Concerning the transconductance, in the case of weak inversion model, it depends linearly on I_D but there is no dependence with β. On the other hand, when strong inversion is considered, the relationship is root-squared and it depends on β.

When relation g_m/I_D is considered, the existing exponential relationship in weak inversion makes this quotient larger, achieving some benefits such as

maximum intrinsic voltage gain and minimum input noise density. Besides, minimum gate voltages are permitted in weak inversion operation, as $V_{GS,wi} < V_{th}$ and the saturation drain voltage is as low as $3U_T$.

The main problem with this technique is that as the bias current is smaller, the speed is also reduced, being the transistor cutoff frequency $f_c \approx \mu_n U_T/(2\pi L^2)$. However, this bandwidth may be enough for some applications, and as it allows very low voltage operation, it can be very beneficial.

2.1.4 Bulk driven transistors

The first paper about bulk driven transistors was published in 1995 [25]. The authors proposed applying the input signal through the bulk terminal instead of the gate terminal of a transistor.

To understand this approach, the behavior of the transistor must be analyzed. The most used model in order to describe the operation of a MOS transistor in strong inversion and saturation is the quadratic law. These formulas are used to perform large-signal analysis. Equations 2.10 and 2.11 define the drain current I_D for triode and saturation region, respectively [26].

$$I_D = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) \cdot V_{DS} \qquad for\ V_{DS} < V_{GS} - V_{TH} \qquad (2.10)$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \qquad for\ V_{DS} \geq V_{GS} - V_{TH} \qquad (2.11)$$

where λ characterizes the channel-length modulation effect. For both regions, the threshold voltage is defined as:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\varphi_F - V_{BS}} - \sqrt{2\varphi_F}\right) \qquad (2.12)$$

being V_{TH0} the zero-bias threshold, φ_F the Fermi potential and γ the parameter corresponding to body effect, all of them dependent on technology.

When the bulk terminal is connected to the source, $V_{TH} = V_{TH0}$, but when there is a voltage difference between these two nodes, V_{BS} has influence on the drain current. If Equations 2.10 and 2.11 are combined with 2.12, the following expressions are obtained:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH0} - \gamma \sqrt{2\varphi_F - V_{BS}} + \gamma \sqrt{2\varphi_F} \right) \cdot V_{DS} \qquad (2.13)$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_{TH0} - \gamma \sqrt{2\varphi_F - V_{BS}} + \gamma \sqrt{2\varphi_F} - \frac{V_{DS}}{2} \right)^2 (1 + \lambda V_{DS}) \qquad (2.14)$$

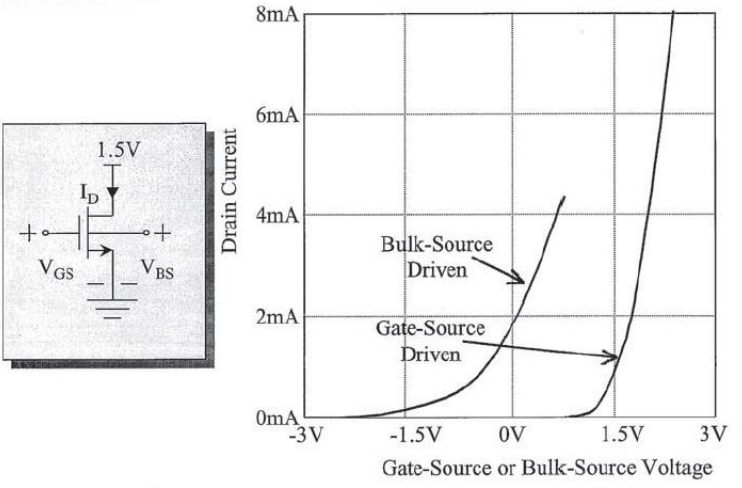


Figure 2.7. Drain current vs bulk-source voltage and gate-source voltage

Thus, when a voltage V_{BS} is present, the threshold voltage can be lowered, thus permitting the transistor to operate with lower voltages. To illustrate this fact clearly, Figure 2.7 is included, which plots the drain current of conventional approach (applying the signal to the gate terminal) and the bulk-driven approach.

However, when other parameters such as gain, output impedance, etc. have to be estimated, a small-signal analysis must be performed. If a transistor operating in the saturation region is considered, there are two transconductances involved, the one from the gate, g_m, and the one from the bulk g_{mb}, defined as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \qquad (2.15)$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{SB}} \qquad (2.16)$$

Once transconductance is defined, the small-signal equivalent circuit is built. Note that parasitic capacitances are not considered in Figure 2.8.

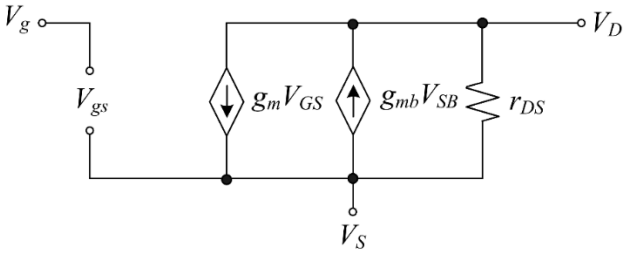


Figure 2.8. Small-signal equivalent circuit of a transistor in saturation region

In the conventional case, the input signal is applied to the gate of the transistor, thus g_{mb} has no influence on the total transconductance. However, when bulk-driven transistors are used, there is a voltage difference between bulk and source terminals, V_{SB}. Therefore, bulk transconductance g_{mb} must be considered in the small-signal equivalent circuit. Equation 2.17 defines the bulk transconductance.

$$g_{mb} = \frac{\partial I_D}{\partial V_{SB}} = \frac{\gamma g_m}{2\sqrt{2\varphi_F - V_{BS}}} \tag{2.17}$$

In theory, bulk transconductance can be greater than the gate transconductance when

$$V_{BS} \geq 2\varphi_F - 0.25\gamma^2 \tag{2.18}$$

However, if this condition is met, there will be a significant current in the p-n union formed by substrate and the source, which can break the device. Thus, to avoid this situation, the value of g_{mb} is normally taken smaller than g_m. The ratio η is defined as the ratio of g_{mb} to g_m, and it typically has a value in the range of 0.2 and 0.4. This may result in lower GBW and worse frequency response, but better linearity and smaller power supply requirements.

This approach also presents some other drawbacks. For conventional gate-driven transistors, the frequency response limitation is described by its transition frequency, f_T.

$$f_{T-GD} = \frac{g_m}{2\pi C_{gs}} \tag{2.19}$$

where C_{gs} is the capacitance between gate and source. In the case of bulk-driven transistors, f_T is given by:

$$f_{T-BD} = \frac{g_{mb}}{2\pi(C_{bs}+C_{bsub})} \tag{2.20}$$

being C_{bs} the capacitance between bulk and source and C_{bsub} the capacitance between bulk and substrate. Capacitance C_{bs} can be comparable to C_{gs}, and C_{bsub} depends on different factors, such as doping density, substrate area, bulk terminal area, etc. The relation between transition frequencies in both cases can be estimated

$$f_{T-BD} \approx \frac{\eta}{3.8} f_{T-GD} \tag{2.21}$$

Another inconvenient of bulk-driven transistors is that the polarity of the bulk-driven MOSFETs is process dependent. For a p-well CMOS process, only N channel bulk-driven transistors are available, and for n-well CMOS process, only P channel. This limits its application. Hence, circuit structures which require both bulk-driven NMOS and PMOS transistors cannot be used in single well processes.

In addition, input equivalent noise of a bulk-driven transistor is larger than a conventional gate-driven MOS amplifier, as its gain is η times the one of conventional case.

2.2 Techniques at circuit level

Whereas Section 2.1 presented different options at device level, this one does so at circuit level. The use of floating voltage sources is going to be introduced in Section 2.2.1, the Flipped Voltage Follower (or FVF) is explained in Section 2.2.2, and finally different adaptive biasing techniques are being proposed in Section 2.2.3.

2.2.1 Use of floating voltage sources

A conventional differential pair amplifier is considered. Figure 2.9(a) presents its schematic. The positive and negative supply voltages are V_{DD} and V_{SS} respectively. If the input pair is formed by NMOS transistors, the input range is $V_{SS} + V_{DSsat5} + V_{GS1,2} < V_{IN} < V_{DD}-V_{SG3}+V_{TH1}$ as shown in Figure 2.9(b).

Similarly, in the case of a PMOS differential pair, the input range is $V_{SS} + V_{GS3} - |V_{TH1}| < V_{IN} < V_{DD} - |V_{DSsat5}| - |V_{GS1,2}|$.

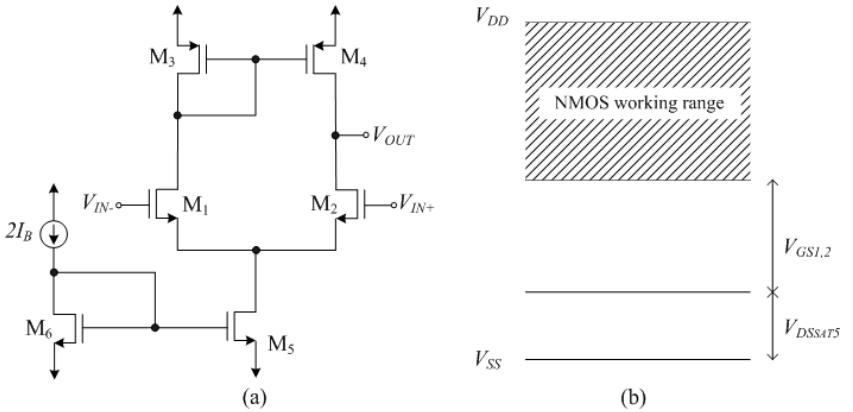


Figure 2.9. NMOS Differential pair (a) Schematic (b) Input range

This amplifier is connected in inverting configuration, as in Figure 2.10. The output signal V_{OUT} is an inverted and scaled version of the input, as the negative input of the amplifier is set to ground by the amplifier feedback. If the DC level of V_{IN} is chosen to be 0 V, only the AC component of V_{IN} will be amplified. Thus, the output voltage can be defined by $V_{OUT} = -(R_2/R_1) \cdot V_{IN}$. Assuming $R_1 = R_2$, $V_{OUT} = -V_{IN}$.

However, the input range does not match the output range, which is a problem.

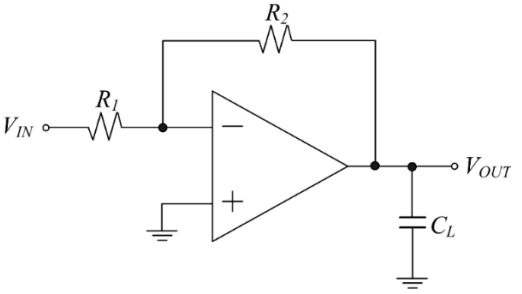


Figure 2.10. Conventional inverting amplifier

To solve this issue and make the input range rail-to-rail, a scheme was proposed in [27] based on the use of a floating voltage source (V_{BAT}) that shifts the DC level to a higher value. The conceptual scheme is shown in Figure 2.11. The positive input terminal of the amplifier is set to V_{DDP}, which is a voltage

near V_{DD}. A floating voltage source is connected between node X and the negative input terminal, whose value is $V_{BAT} = V_{DDP}$. The op-amp forces the negative input terminal to be V_{DDP}, and thanks to the floating voltage source, voltage at node X is 0 V, thus the same DC level given by the input voltage source and the output node. Therefore, the behavior in the feedback loop is the same as in conventional approach, but the gate voltage of the differential input pair is set to V_{DDP}, making the DC operating point more convenient, avoiding the limitation of the input range and making it possible to use rail-to-rail signals.

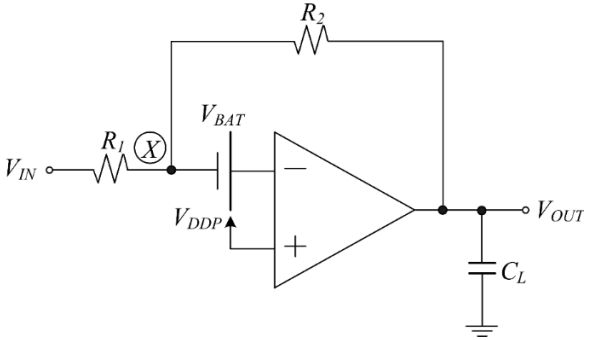


Figure 2.11. Low-voltage approach by using a floating voltage source [27]

There are different ways of implementing the DC level shifter. A simple approach is to utilize a resistance R_{BAT} with a DC current I_{BAT} through it, causing a voltage difference between its nodes V_{BAT}, fulfilling Ohm's law $V_{BAT} = R_{BAT} \cdot I_{BAT}$. This topology is shown in Figure 2.12 [28].

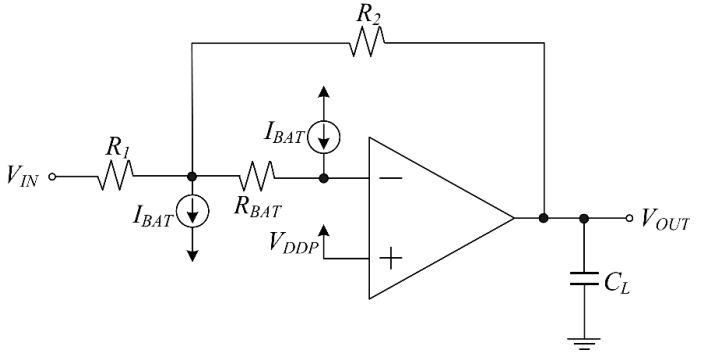


Figure 2.12. Low-voltage amplifier with R_{BAT} acting as floating voltage source [28]

A possible implementation of the current sources is shown in Figure 2.13 [28]. The one connected to V_{DD} that generates I_1 is a single transistor,

since V_{DDP} is a voltage close to V_{DD}. A cascode NMOS current source generates I_2. It is required that $I_1 = I_2 = I_{BAT}$.

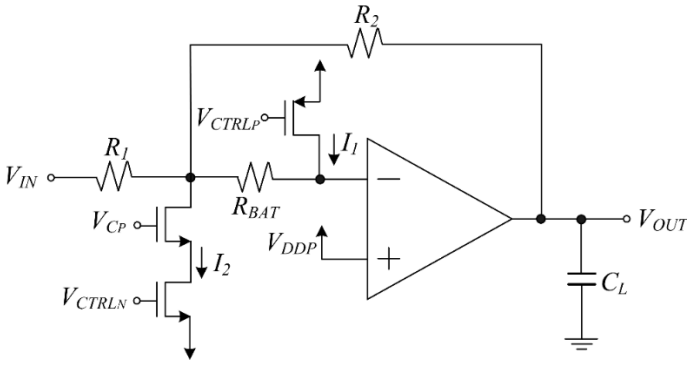


Figure 2.13. Low-voltage amplifier with transistors as current sources [28]

In order to create the gate voltages of these transistors, V_{CNTP} and V_{CNTN} respectively, an auxiliary circuit is needed. It is shown in Figure 2.14. It is formed by a conventional differential pair and a second stage composed by two branches biased by the same current I_{BAT}. The reason why these currents I_1 and I_2 are fixed to I_{BAT} is explained in the following paragraph.

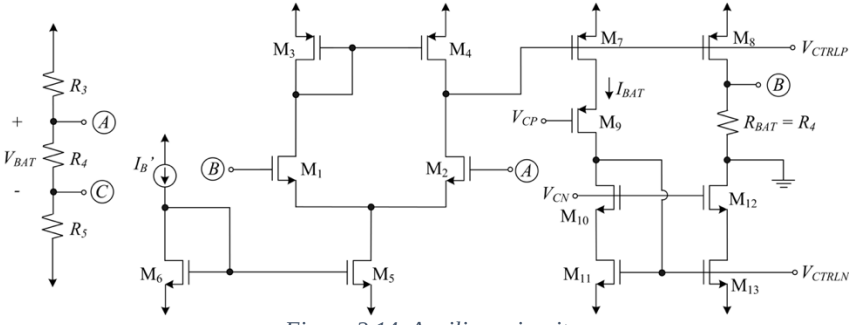


Figure 2.14. Auxiliary circuit

V_{DDP} is obtained through a resistive divider formed by three resistors whose values are R_3, R_4 and R_5. In this way, node A has a value of V_{DDP} and node C is set to 0 V, because conditions $V_{DDP} = (R_4V_{DD})/(R_3 + R_4)$ and $R_3 + R_4 = R_5$ are imposed as a design requirement. Thus, resistance R_2 has a voltage drop of V_{DDP}. Node A is connected to the negative input of the differential pair, which forces node B to be also V_{DDP}. As resistor $R_{BAT} = R_4$ is connected to B and ground, the voltage drop through these nodes is $V_{BAT} = V_{DDP}$, fixing the current of the output branches to I_{BAT}. Note that the second stage has

to be well designed, as some current can go through the ground terminal, leading to a mismatch between the currents I_1 and I_2 in Figure 2.13, which would lead to an offset in the output signal.

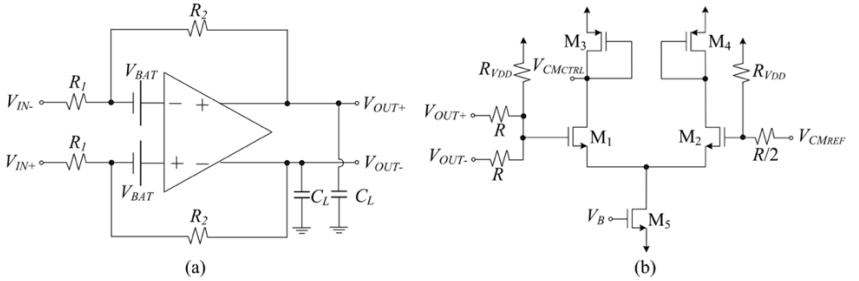


Figure 2.15. Fully differential configuration (a) Low-voltage amplifier (b) CMFB circuit

This technique can also be applied to fully differential configurations, as Figure 2.15(a) illustrates. Besides the auxiliary circuit, a common mode feedback (CMFB) circuit is needed in order to control the common mode (CM) voltage of the output signal. The CMFB circuit is displayed in Figure 2.15(b). It is similar to the conventional CMFB circuit but it adds two resistors, R_{VDD}, connected to V_{DD} in order to pull the DC level up until it reaches a value of V_{DDP}. Resistors R_{Vdd} should be smaller than resistors R, so that the voltage at the gates of M_1 and M_2 are close enough to V_{DD}.

A second approach in order to operate in low-voltage mode using constant floating voltage sources is using capacitors instead of resistors to create the feedback loop. Figure 2.16(a) presents the conventional inverting stage, and Figure 2.16(b), the low voltage scheme [29]. The voltage gain of the amplifier in both cases is $G_{IL}=-C_{IN}/C_f$. As it happened in the previous case, this option is not suitable for low power applications, because input range limits the amplitude of the signal, avoiding to process rail-to-rail signals. This issue can be solved by connecting a large resistor (R_{large}) and a constant floating voltage source between the negative input and the output of the amplifier. In DC, capacitors behave as open circuits, thus the DC component of the input is blocked. Besides, the DC voltage of the input pair is V_{DDP}, which allows the input signal to work with bigger amplitudes in addition of maintaining the output DC level to 0 V, as $V_{BAT} = V_{DDP}$. The purpose of using R_{large} is to ensure that the majority of the AC current goes to the branch of C_f to be amplified. This large resistor can be implemented by a diode-connected transistor, as explained in Section 2.1.2, and the floating voltage source V_{BAT} by the same circuit as before.

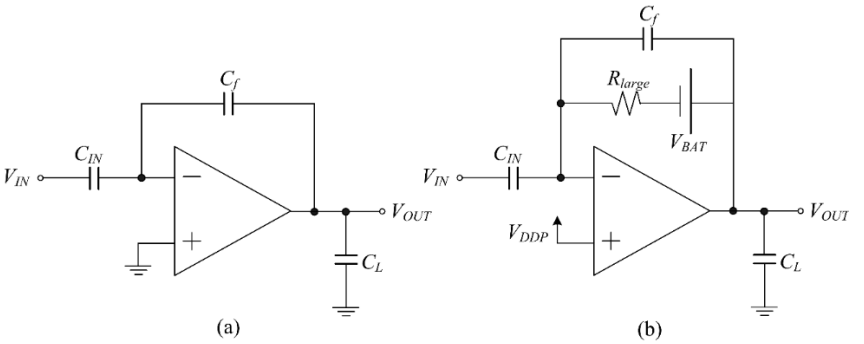


Figure 2.16. Capacitive amplifier (a) Conventional configuration (b) Low-voltage approach [29]

As it was said in the previous paragraph, the DC component of V_{IN} is filtered out due to capacitor C_{IN}. This is an advantage, because in case there is a little offset between the input terminals, it is not amplified. Nevertheless, it also presents a drawback. When a load capacitor is connected to the output, there is a capacitive divider that attenuates the gain, following the expression:

$$G|_{HF} = \frac{\frac{C_{IN}C_f}{C_{IN}+C_F}}{\frac{C_{IN}C_f}{C_{IN}+C_f}+C_L} = \frac{C_f}{C_f+C_L} \tag{2.22}$$

This topology can be applied to a fully differential amplifier, as it is illustrated in Figure 2.17. Note that same CMFB circuit than in Figure 2.15 is required.

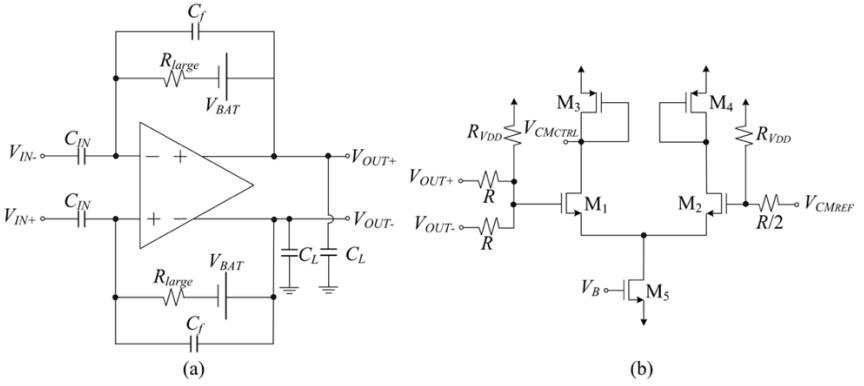


Figure 2.17. (a) Fully differential version of capacitive inverting amplifier (b) CMFB circuit

2.2.2 The Flipped Voltage Follower (FVF)

The voltage follower is a block that is commonly used when designing analog circuits. It is in charge of copying the input voltage at its output. The input impedance should be high, while it must present low output impedance to drive low resistive or high capacitive loads. Besides, it must copy the voltage between its terminals accurately.

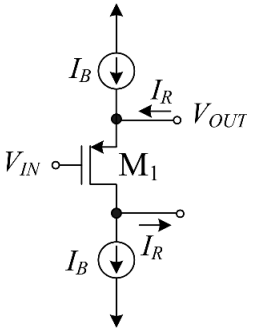


Figure 2.18. Source follower

The simplest existing implementation and the most widely used one is the source follower (SF). This circuit is really fast because it does not have a feedback loop in its design. However, it is not very linear. According to Figure 2.18, the input signal is connected to the high-impedance gate, and the output signal, $V_{OUT} = V_{IN} - V_{GS1}$, is obtained at the low-impedance source terminal. However, the voltage transfer from the input voltage to the output terminal is inaccurate, because the current through M_1 is dependent on the input signal, making V_{GS1} also signal dependent. This problem is unavoidable, as transistor M_1 sets the output voltage and at the same time, it drives the load. As a consequence, there is a small-signal gain, as well as an output resistance (its value is around a few kΩ), estimated in Equations 2.23 and 2.24.

$$A_v = \frac{V_{OUT}}{V_{IN}} = \frac{1}{1+\frac{g_{mb1}}{g_{m1}}+\frac{1}{g_{m1}R_L}} < 1 \tag{2.23}$$

$$r_{out} = \frac{1}{g_{m1}+g_{mb1}} \tag{2.24}$$

with g_{m1} and g_{mb1} the transconductance and backgate transconductance of transistor M_1, respectively. To make term g_{mb1} disappear, transistor can be fabricated in an independent well tied to its own source. If g_{m1} increases, linearity will improve and r_{out} will decrease. To do so, large bias currents and widths of the transistor are needed, thus increasing the area and power

dissipation. For that reason, this topology is not a good option for modern very large-scale integration deep-submicrometer CMOS processes with low supply voltages [30].

A possible alternative to source follower is the flipped voltage follower, or FVF [31], [32], shown in Figure 2.19.

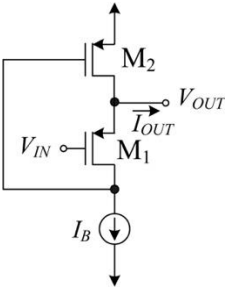


Figure 2.19. Flipped Voltage Follower

In this topology, a second transistor M_2 is used to create a negative feedback loop. This transistor drives the load, relieving M_1 from that task. Now, M_1 is biased with a constant current, setting the output voltage optimally. This causes an improvement in linearity and a reduction in the output resistance.

$$r_{out} = \frac{1}{(g_{m1}+g_{mb1})g_{m2}(r_{o1}\|r_{B1})} \tag{2.25}$$

being r_{o1} the drain-source resistance of M_1 and r_{B1} the output resistance of the current source I_{B1}. The value of this output resistance is a few Ohms, in contrast with the one obtained at the SF, which was in the order of a few kΩ. If channel length modulation and body effect are neglected, current through M_1 and voltage V_{GS1} become constant, improving linearity.

As for the stability of the FVF cell, transistor M_2 provides shunt feedback, forming a two-pole negative feedback loop. To ensure its stability, transistors must be properly sized so that condition $g_{m1}/4g_{m2} > C_{p1}/C_{p2}$ is fulfilled, with C_{p1} and C_{p2} the parasitic capacitances at the source and drain of M_1, respectively. Note that C_{p1} includes the FVF load capacitance. For large FVF capacitive loads, C_{p2} can be increased by adding a grounded compensation capacitor at the drain of M_1.

Despite being widely used in low-voltage applications, the FVF has important disadvantages. The main one is that the drain voltage of M_1 is fixed to that of the gate of M_2, limiting the input voltage range, which is independent

of the supply voltage. This range is given by $|V_{TH1}|$ - $|V_{DS1sat}|$, with V_{DS1sat} the drain-source saturation voltage of M_1 and V_{th1} its threshold voltage, which depends strongly on the fabrication technology. Its value can be very small in modern deep-submicron processes. In order to solve this drawback, a DC level shift can be included in the FVF loop, e.g. using a source follower biased by a constant current.

2.2.3 Adaptive Biasing Techniques

As it was said in the introduction of this chapter, in order to decrease the static power dissipation, either bias current or supply voltages must be reduced. However, if a classical biasing scheme is used to design an amplifier, its slew rate will be limited, as limitation in this parameter is a consequence of a fixed tail current source. This problem can be solved by adding an extra input-dependent tail current source, thus obtaining a higher slew-rate. This idea was introduced by [33] in 1982. It was coined as "Adaptive Biasing" technique, and since then, a lot of different topologies have been proposed based on this concept.

In this subsection, some of these schemes are introduced, classified in two groups: adaptive biasing techniques applied to the input stage, i.e. to the input differential pair, or to the load stage.

2.2.3.1 Applied to the input stage

• *Cross-Coupled Floating Batteries*

One approach in order to obtain adaptive biasing techniques is the use of two matched transistors M_1 and M_2, forming the input differential pair, cross-coupled by two DC level shifters [34]-[36]. The conceptual scheme is drawn in Figure 2.20(a). Under quiescent conditions, $V_{SG1}^{Q} = V_{SG2}^{Q} = V_B$, therefore quiescent current through transistors M_1 and M_2 are the same and they are controlled by V_B. Very low standby currents can be created if the value V_B is chosen slightly larger than $|V_{TH}|$. Nevertheless, when V_{in+} decreases, the same voltage decrease is experienced at the source of M_1, while the voltage at the source of M_2 remains invariable. Thus, I_2 increases whereas I_1 is reduced. These currents can achieve values much larger than the quiescent current. As for the implementation of the DC level shifters, they should present very low output impedance, they must have the capacity of sourcing/sinking large currents to

charge and discharge large load capacitances, and they also should be simple to avoid penalties in noise, speed and minimum supply voltages.

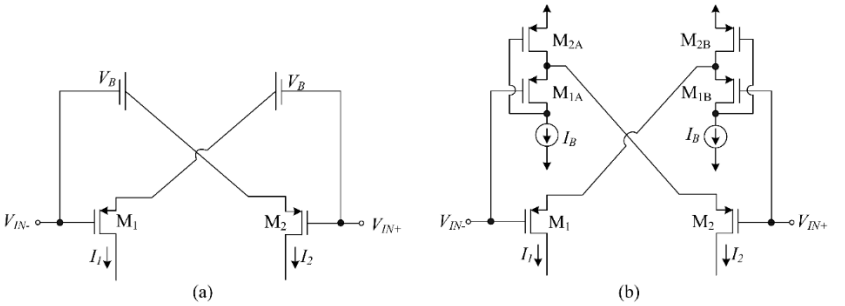


Figure 2.20. Adaptive basing topology by two level shifters (a) Diagram (b) Implementation

A very good choice is the use of two Flipped Voltage Followers, as Figure 2.20(b) shows [35], [36]. This block was explained in Section 2.2.2. In quiescent conditions and assuming that M_1, M_2, M_{1A} and M_{2A} are matched, current through M_1 and M_2 are the well-controlled bias current I_B of the FVFs. When a differential input signal is applied, currents I_1 and I_2 verify Equations 2.26 and 2.27, respectively.

$$I_1 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} + V_{id}\right)^2 \qquad I_2 < I_B \quad V_{id} > 0 \tag{2.26}$$

$$I_2 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} - V_{id}\right)^2 \qquad I_1 < I_B \quad V_{id} < 0 \tag{2.27}$$

When transistors M_1 and M_2 operate in strong inversion and saturation, differential current I_d is defined by $I_d = I_1 - I_2 = \sqrt{(8\beta_{1,2}I_B)}\cdot V_{id}$. However, $V_B - |V_{TH}| = \sqrt{(2I_B/\beta_{1,2})}$ has such a small value that causes the input transistor with the lowest V_{SG} to be driven out of strong inversion for small values of V_{id}, thus I_d soon becomes dependent on V_{id}^2. When this happens, differential current is $I_d = I_1 - I_2 \approx I_1$ and common-mode current is $I_{cm} = (I_1 + I_2)/2 \approx I_1/2$ for large positive V_{id} while $I_d \approx -I_2$ and $I_{cm} \approx I_2/2$ for large negative V_{id}. Therefore, it can be deduced from Equations 2.26 and 2.27 that I_1 and I_2 are not limited by I_B, achieving class AB operation. Besides, the common-mode current I_{cm} is dependent on the input signal, as in other class AB topologies.

In addition, the transconductance of the input stage is doubled compared with the conventional differential pair, because the AC input signal is

applied to both the gate and the source terminals of M_1 and M_2. This fact is also reflected in the small signal differential current, according to Equation 2.28.

$$i_d = i_1 - i_2 \approx \left(1 + \frac{g_{m2A,B} r_{o1A,B} - 1}{g_{m2A,B} r_{o1A,B} + 1}\right) g_{m1} v_{id} \approx 2 g_{m1} v_{id} \qquad (2.28)$$

While other approaches based on source-coupled nMOS and pMOS transistors need a minimum supply voltage of $2|V_{TH}| + 3|V_{DS,sat}|$ [37], the minimum supply voltage of this circuit is $|V_{TH}| + 3|V_{DS,sat}|$. However, the FVF is only suitable to low supply voltages, as the drain voltage of $M_{1A,B}$ is $V_{DD} - V_{SG2A,B}$. If V_{DD} is large enough, that voltage can force $M_{1A,B}$ to enter triode region. To avoid this issue, as mentioned in Section 2.2.2, a DC level shifter can be included in the FVF loop. To implement it, a source follower can be employed [31].

• *Pseudodifferential Pair*

Figure 2.21(a) shows the following alternative class AB input stage [34], [38], [39]. The input common-mode voltage, V_{cm}, shifted by V_B is applied to the common-source node of the input differential pair. Under quiescent conditions, $V_{SG1}^Q = V_{SG2}^Q = V_B$ and the quiescent currents are controlled by voltage V_B, as it happened in Figure 2.20(a). When a differential signal exists between the input terminals, drain current becomes unbalanced, which is not limited by the quiescent current.

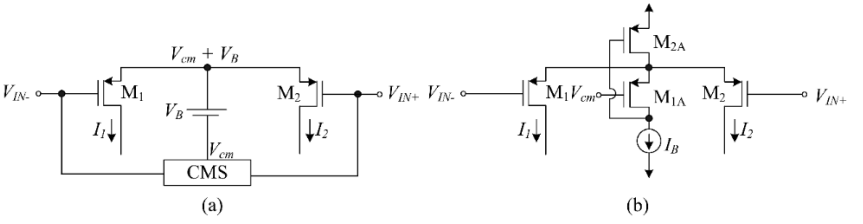


Figure 2.21. Adaptive biasing topology using CMS (a) Diagram (b) Implementation

The DC level shifter is implemented by a FVF due to its efficiency. Figure 2.21(b) presents the resulting circuit. As it can be deduced from this figure, $V_B = V_{SG1A}$ and the quiescent current of the input differential pair is the FVF bias current I_B (assuming that M_1, M_2 and M_{1A} are matched). Expressions 2.29 and 2.30 define currents I_1 and I_2.

$$I_1 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} + \frac{V_{id}}{2}\right)^2 \qquad I_2 < I_B \quad V_{id} > 0 \tag{2.29}$$

$$I_2 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} - \frac{V_{id}}{2}\right)^2 \qquad I_1 < I_B \quad V_{id} < 0 \tag{2.30}$$

As in the previous case, there is a quadratic dependence on the output currents with V_{id} and they are not limited by I_B. A CMS (common-mode sensor) is needed in order to sense the common-mode input voltage V_{cm} and to apply it to the gate of transistor M_{1A}. The purpose of this block is to make quiescent current independent of the input common-mode voltage, hence obtaining a high common-mode rejection ratio (CMRR).

However, the small-signal transconductance of the input stage is the same as in the conventional approach, as the AC input signal is only applied to the gate of the input transistors and their source is an AC virtual ground. Thus, there is no increase in g_m.

A positive feature of this adaptive biasing technique is that it presents the same supply voltage requirements and common-mode input range as for the case with DC level shifters, making it suitable for low-voltage applications.

• *Winner-take-all Input Stage*

If the CMS circuit of Figure 2.21(a) is replaced by a Winner-Take-All (WTA) block, the topology shown in Figure 2.22(a) is obtained [34].

The output voltage of the WTA circuit is the "winner", i.e. the maximum, of the input voltages. This voltage shifted by V_B is applied to the voltage at the common-source node of the differential pair. Under quiescent conditions, both inputs have the same value, so their maximum value is the common-mode input voltage. Hence, $V_{SG1}^Q = V_{SG2}^Q = V_B$ and this value controls the quiescent currents, like in Figure 2.20(a) and Figure 2.21(a). However, under dynamic conditions, if for instance, V_{in+} decreases, the common-source node tracks V_{in-}, achieving larger V_{SG2} and thus, a larger dynamic current boosting.

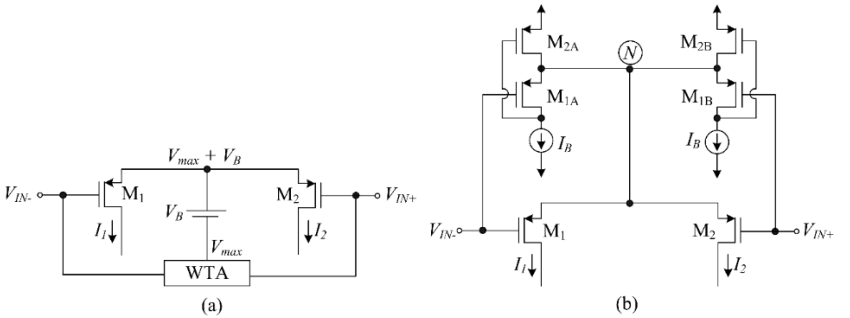


Figure 2.22. Adaptive biasing topology using WTA (a) Diagram (b) Circuit

An efficient way of implementing the WTA is described in Figure 2.22(b). The FVF cell is employed once again. Assuming that M_1, M_2, M_{1A} and M_{2A} are matched, $V_{in+} = V_{in-} = V_{cm}$ under quiescent conditions, and voltage at node *N* is $V_N = V_{cm} + V_B = V_{cm} + V_{SG1A}$, setting the quiescent current to I_B. When for instance V_{in-} decreases, V_{SG1A} increases, so as the drain voltage of M_{1A}, making transistor M_{1A} to enter into triode region. Voltage at node *N* is $V_N = V_{in+} + V_{SG1B}$, thus depending on V_{in+}, current I_B and the dimensions of M_{1B}. On the contrary, when V_{in-} increases, $V_N = V_{in-} + V_{SG1A}$.

For positive V_{id}, currents I_1 and I_2 are defined by:

$$I_1 = \frac{\beta_{1,2}}{2}(-V_{in-} + V_N - |V_{TH}|)^2 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} + V_{id}\right)^2 \quad (2.31)$$

$$I_2 = 0 \quad (2.32)$$

If V_{id} is negative, currents through M_1 and M_2 are:

$$I_2 = 0 \quad (2.33)$$

$$I_2 = \frac{\beta_{1,2}}{2}(-V_{in+} + V_N - |V_{TH}|)^2 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} - V_{id}\right)^2 \quad (2.34)$$

Transconductance of this stage is the same as using the CMS circuit, thus no improvement is achieved because node *N* is an AC virtual ground.

2.2.3.2 Applied to the load stage

• *Local Common-Mode Feedback (LCMFB) configuration*

This topology was proposed by [40] in order to achieve class AB operation. In this article, the load stage was rearranged thanks to the use of two

matched resistors to provide better performance to the amplifier. In the following paragraphs, this technique will be explained.

The conventional class A symmetrical amplifier is represented in Figure 2.23(a). Note that the aspect ratio of transistors M_5 and M_8 is B times that of M_6 and M_7, forming two current mirrors with current gain B. The DC open-loop gain is $A_{OL} = Bg_{m1,2}R_{out}$ and the dominant pole is at $f_{Pout} = 1/(2\pi R_{out}C_L)$, with $g_{m1,2}$ the transconductance of M_1 and M_2, R_{out} the output equivalent resistance and C_L the capacitance at the output node. Hence, the gain-bandwidth product is GBW = $B{\cdot}g_{m1,2}/(2\pi C_L)$. The internal poles at nodes X and Y are $f_{PX} \approx g_{m6}/(2\pi C_X)$ and $f_{PY} \approx g_{m7}/(2\pi C_Y)$, respectively, where C_X and C_Y are the parasitic capacitances at nodes X and Y, and they can be estimated as $C_X \approx C_{gs5} + C_{gs6}$ and $C_Y \approx C_{gs7} + C_{gs8}$.

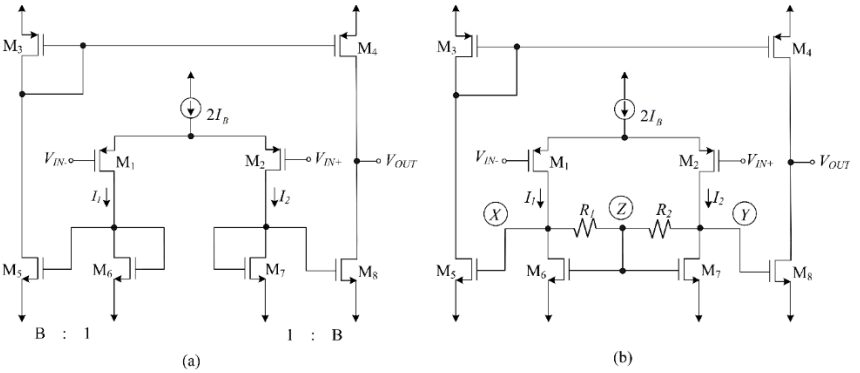


Figure 2.23. (a) Conventional class A amplifier (b) Class AB amplifier with LCMFB

The quiescent current through transistors M_1, M_2, M_6 and M_7 is I_B whereas that of M_3, M_4, M_5 and M_8 is $B{\cdot}I_B$. The slew rate is SR = $2{\cdot}B{\cdot}I_B/C_L$, as the maximum output current is $2{\cdot}B{\cdot}I_B$. In order to get large SR values, either the bias current I_B or factor B should be large. An increase in I_B causes an increase in static power dissipation. Factor B can be increased, leading to an improvement in slew rate, GBW and current efficiency, which is given by $CE = B/(B + 1)$. However, if the current mirrors are operating in strong inversion, the static current consumption is $I_Q = SR{\cdot}C_L{\cdot}(1+1/B)$, hence the slew rate is only increased proportionally to the static power consumption, as quiescent currents suffer the same multiplication factor B as dynamic currents do. In addition, larger parasitic capacitances at nodes X and Y are obtained with larger B, causing a reduction in phase margin (PM). Typically, value B is set to 1.

In order to achieve class AB operation, the active load is modified following a local common-mode feedback (LCMFB) topology [40], [41]. Two matched resistors R_1 and R_2 are connected in series between the drains of transistors M_6 and M_7. The node between R_1 and R_2 extracts the common-mode voltage of these drain nodes, which is fed back to the common gate of M_6 and M_7.

If an AC small-signal differential voltage v_{id} is applied to the input, complementary small signal currents i_1 and i_2 are created, fulfilling $i_1 = -i_2 = g_{m1,2}v_{id}/2$. If $R_{1,2} << r_{o6,7}$, with $r_{o6,7}$ the small-signal drain-source resistance of M_6 and M_7, there is a small-signal current $i_R = i_1 = -i_2$ flowing through resistors R_1 and R_2, creating complementary AC voltage variations at nodes X and Y ($v_x = -v_y = R_{1,2} \cdot i_R = R_{1,2}g_{m1,2}v_{id}/2$). Thus, node Z becomes an AC virtual ground, as $v_Z = 0$. This causes that the parasitic C_{gs6} and C_{gs7} have no influence in the capacitance of nodes X and Y, increasing the high-frequency poles f_X and f_Y. However, resistors $R_{1,2}$ make the small-signal resistance at these nodes to increase ($R_{X,Y} \approx R_{1,2} \| r_{o6,7} \| r_{o1,2}$). Hence, there is a tradeoff between DC gain and phase margin. The gain-bandwidth product is defined in Equation 2.35. There is an increase factor of $g_{m5,6} \cdot R_{X,Y}$ versus conventional class A amplifier.

$$GBW = \frac{g_{m1,2}g_{m5,8}R_{X,Y}}{2\pi C_L} \tag{2.35}$$

When the differential input signal is null, currents I_1 and I_2 in Figure 2.23(b) have the same value I_B, and there is no current flowing though resistors R_1 and R_2. Thus, voltage at nodes X, Y and Z is defined by:

$$V_X = V_Y = V_z = V_{TH} + \sqrt{\frac{2I_B}{\beta_{6,7}}} \tag{2.36}$$

However, when a non-zero differential input signal $V_{id} = V_{i+} - V_{i-}$ is applied, this differential voltage causes a differential current $I_d = I_1 - I_2$ that leads to a current in the resistors $I_R = I_d/2 = (I_1 - I_2)/2$. The common-mode current $I_{cm} = (I_1 + I_2)/2$ flows through M_6 and M_7, thus the nodal voltages are:

$$V_Z = V_{TH} + \sqrt{\frac{2I_{cm}}{\beta_{6,7}}} \tag{2.37}$$

$$V_X = V_Z + \frac{R_1 I_d}{2} \tag{2.38}$$

$$V_Y = V_Z - \frac{R_2 I_d}{2} \tag{2.39}$$

Therefore, for positive differential input voltages (V_{id} > 0V), node *X* experiences a large positive swing. Assuming that M_5 operates in strong inversion and saturation, current through this transistor is:

$$I_5 = \frac{\beta_5}{2}\left(V_Z + \frac{R_1 I_d}{2} - V_{TH}\right)^2 = \frac{\beta_5}{2}\left(\sqrt{\frac{2I_{cm}}{\beta_{6,7}}} + \frac{R_1 I_d}{2}\right)^2 \quad (2.40)$$

On the other hand, current through M_8 strongly decreases due to the large negative swing at node *Y*, even below I_B. Hence, the output current is $I_{out} = I_5 - I_8 \approx I_5$. Consequently, for negative differential input signals, the large positive swing happens at node *Y*, causing a large current in I_8:

$$I_8 = \frac{\beta_8}{2}\left(V_Z - \frac{R_2 I_d}{2} - V_{TH}\right)^2 = \frac{\beta_8}{2}\left(\sqrt{\frac{2I_{cm}}{\beta_{6,7}}} - \frac{R_2 I_d}{2}\right)^2 \quad (2.41)$$

In this case, I_5 is negligible, so $I_{out} = I_5 - I_8 \approx -I_8$. Taking this into account, a general equation for the output current is:

$$I_{out} = I_5 - I_8 \approx \pm\frac{\beta_{5,8}}{2}\left(V_Z + \frac{R_{1,2}|I_d|}{2} - V_{TH}\right)^2 = \pm\frac{\beta_{5,8}}{2}\left(\sqrt{\frac{2I_{cm}}{\beta_{6,7}}} + \frac{R_{1,2}|I_d|}{2}\right)^2 \quad (2.42)$$

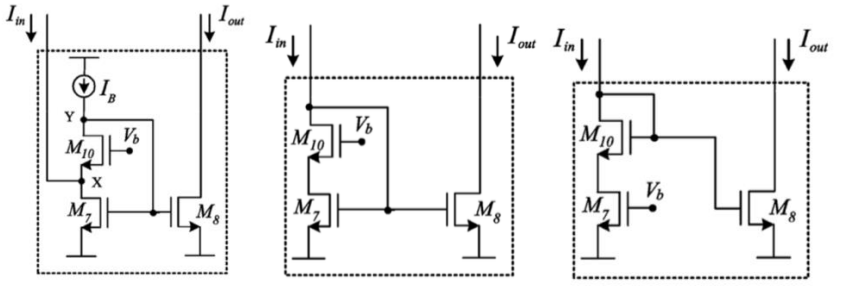
An approximate expression for current efficiency is:

$$CE = \frac{|I_{out}|}{|I_{out}| + 2I_{cm}} = \frac{1}{1 + \frac{2I_{cm}}{|I_{out}|}} \quad (2.43)$$

Under dynamic conditions, $|I_{out}| >> I_{cm}$, thus current efficiency is almost 1, whereas that of conventional class A amplifier is 0.5 for B =1.

• *Nonlinear Current Mirrors*

Other alternative in order to obtain the desired output current boosting is the implementation of nonlinear current mirrors. Such nonlinearity is achieved by the transition between the ohmic and saturation region of some of the transistors of the current mirror. Expressions 2.10 and 2.11 define the drain current of a MOSFET in triode and saturation region, respectively. Figure 2.24 shows some nonlinear current mirrors that were proposed in [41].



(a) (b) (c)

Figure 2.24. Nonlinear current mirrors (a) Based on FVFCS (b) Based on FVFs (c) Based on Source Degeneration MOS Resistors

The first option, shown in Figure 2.24(a), uses the scheme known as FVF current sensor (FVFCS). If all transistors are working in the saturation region, the output of this stage is $I_{out} = I_{in} + I_B$. If transistor M_7 is biased near the linear region and M_8 is maintained in the saturation region, the output current can be increased several times compared to the input current, following the expression:

$$I_8 = \frac{\beta_8}{2}\left(\frac{I_{in}+I_B}{\beta_7 V_{DS7}}\right)^2 \tag{2.44}$$

where V_{DS7} is set by the current source I_B and voltage V_b. Figure 2.25 shows the comparison between the output currents when M_7 is in saturation (dotted line) or in ohmic region (continuous line).

Besides the increase in output current, there is an enhancement on the total transconductance of the OTA, thus increasing GBW and the slew rate accordingly. This fact is caused by $M_{6,7}$ entering in triode region, since their transconductance decreases [41].

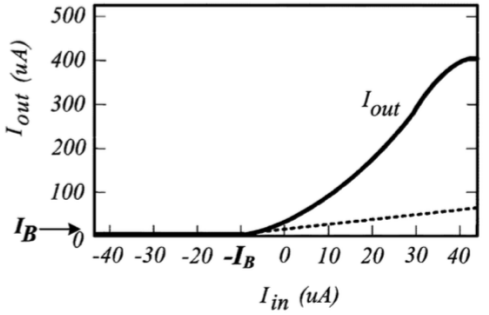


Figure 2.25. Comparison between conventional and nonlinear FVFCS current mirror (extracted from [41])

Figure 2.24(b) presents a nonlinear current mirror based on FVFs. Transistor M_7 must be biased near the ohmic region, so that when I_{in} increases, V_{DS7} decreases, thus driving it to the ohmic region, boosting the output current as long as M_8 remains in saturated mode. This time, drain current through M_8 is:

$$I_8 = \frac{\beta_8}{2}\left(\frac{I_{in}}{\beta_7 V_{DS7}}\right)^2 \tag{2.45}$$

being V_{DS7} dependent on V_b and the input current I_{in}. Like in the previous case, GBW and slew rate increase when M_7 operates in ohmic region, since there is a decrease in its transconductance.

Last, the third topology of a nonlinear current mirror in Figure 2.24(c) is based on source degeneration MOS resistors. The difference versus the previous cases is that M_7 is biased in ohmic region by a constant gate voltage, but near the boundary of saturation region. When the drain current I_{in} of M_7 increases, it enters saturation, yielding a very large drain-source saturation voltage. Thus, there is a large increase in the gate-source voltage of M_8, leading to a large increase in the output current, expressed by:

$$I_8 = \frac{\beta_8}{2}\left(\sqrt{\frac{2I_{in}}{\beta_{10}}} + \frac{2I_{in}}{\lambda_7\beta_7(V_b - V_{TH})^2} - \frac{1}{\lambda_7}\right)^2 \tag{2.46}$$

with $\lambda \neq 0$ and $V_b > V_{th}$.

2.3 Conclusions

This chapter summarizes some of the techniques employed in order not only to obtain low voltage and low power circuits, but also to maximize the performance of the blocks. Moreover, some applications have been presented, making use of different techniques. Focus has been on QFGMOS transistors, adaptive biasing techniques and LCMFB, which will be employed in this thesis.

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Chapter 3

SUBTHRESHOLD LOGIC FAMILY

A logic gate is an electronic device that implements a Boolean function. Signals are represented as “0” or “1”, despite being electronic voltages. There are different logic gates, depending on the Boolean function that they perform. These gates are grouped into logic families, each one with its own distinctive features. Nowadays, the most used logic family is the CMOS one, due to its very low static consumption and adaptability to the dominant CMOS technologies. However, conventional operation of CMOS transistors requires supply voltage above their threshold voltage. In early 1970s, [1] made great advances based on subthreshold operation. Since then, different analog subthreshold circuits were developed for low-power applications [2], [3]. However, digital subthreshold circuits did not receive the same interest until the late 1990s [4]-[6]. These proposals often used body biasing, which is often not convenient, since the severe reduction of the supply voltage causes a strong performance degradation: the delay of the circuits increases exponentially and the leakage becomes very relevant [7].

In this Chapter, a new subthreshold logic family is proposed, based on QFG [8] transistors which were presented in the previous chapter, in order to decrease the supply voltage. Setting the DC gate voltage of a QFG transistor to a supply rail, the input capacitive coupling allows shifting this gate voltage above the positive supply rail or below the negative supply rail. This way, the pull-up or pull-down output transistors of a CMOS logic gate can be operated even with supply voltages well below the threshold voltage V_{TH}. Since $V_{DD}<|V_{TH}|$, and due to the attenuation of such capacitive coupling, the peak

voltage over (or below) the supply rail in the QFG gate is never larger than $0.5V_{TH}$, so the reverse p-n junction that isolates the drain and source terminals from the bulk is not forward biased.

In particular, the design of four logic gates will be addressed in this Chapter. Section 3.1 presents the QFG CMOS inverter. In Section 3.2, the QFG MOS NAND, NOR and XOR logic gates are explained. Two applications of these improved logic gates are included in Section 3.3: a ring oscillator and a clock doubler. Finally, some conclusions are drawn in Section 3.4.

3.1 QFG CMOS Inverter

The schematic of the proposed QFG CMOS inverter is shown in Figure 3.1. It employs a 1-input QFG pMOS transistor M_P whose DC gate voltage is set to $V_{GMP,DC} = V_{SS}$ by the large resistance of a minimum-size transistor $M_{Rlarge1}$ in cutoff region, and whose AC voltage $V_{GMP,AC}$ results from the AC input voltage applied to the capacitive divider formed by C_P and the parasitic capacitance at the gate of M_P, i.e., $V_{GMP,AC} = a_P V_{IN,AC}$ where $a_P \approx C_P/(C_P+C_{GS,MP})$. Since V_{IN} is a square waveform swinging from V_{DD} to V_{SS}, $V_{IN,AC} = \pm V_{DD}/2$ (assuming $V_{SS} = 0$ V), so when $V_{IN} = 0$ V, $V_{GMP,AC} = -a_P V_{DD}/2$ and $V_{SG,MP} = (1+a_P/2)V_{DD}$. Choosing C_P sufficiently larger than $C_{GS,MP}$, $V_{SG,MP} \approx 1.5V_{DD}$ and the pMOS transistor can provide a relatively large current to the output node even with $V_{DD}<|V_{TH}|$. Similarly, the 1-input QFG nMOS transistor M_N has a DC voltage $V_{GMN,DC} = V_{DD}$ set by the large resistance of a transistor $M_{Rlarge2}$ in cutoff region, and AC voltage $V_{GMN,AC} = a_N V_{IN,AC}$ where $a_N \approx C_N/(C_N+C_{GS,MN})$. Choosing C_N sufficiently larger than $C_{GS,MN}$, when $V_{IN} = V_{DD}$, $V_{GS,MN} \approx 1.5V_{DD}$ and the nMOS transistor is able to collect a relatively large current from the output node.

The achievement of $|V_{GS}|>V_{DD}$ in the output transistors allows operation with $V_{DD}<|V_{TH}|$ generating much larger output currents than when $|V_{GS}|$ is limited to V_{DD} and thus suffering from less speed degradation than conventional logic operating in subthreshold region.

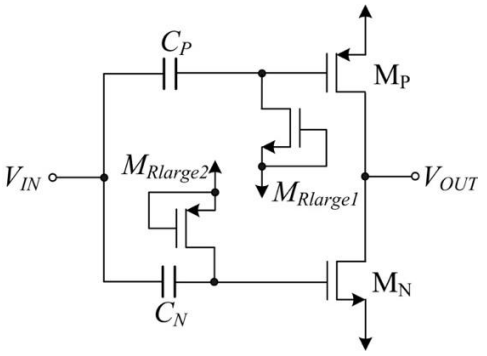


Figure 3.1. NOT logic gate using QFG transistors

By using this improvement, the minimum supply voltage can be reduced, in exchange of a larger die area. A 0.5 µm CMOS technology with nominal NMOS and PMOS threshold voltages of 0.67 V and -0.96 V, respectively, has been used to implement the whole family of logic gates. Note the large threshold voltage values, which preclude very low voltage operation using conventional CMOS logic.

The simulated Voltage Transfer Characteristics (VTC) of a standard CMOS inverter in this technology for a supply voltage ranging from 0 to 2 V in 0.1 V steps are plot in Figure 3.2. Note that the inverter cannot operate properly below 0.4 V. In the range from 0.4 V to about 0.9 V, despite the DC transfer characteristics are correct, dynamic operation is limited since transistors operate in weak inversion and deliver very low currents, leading to slow transients.

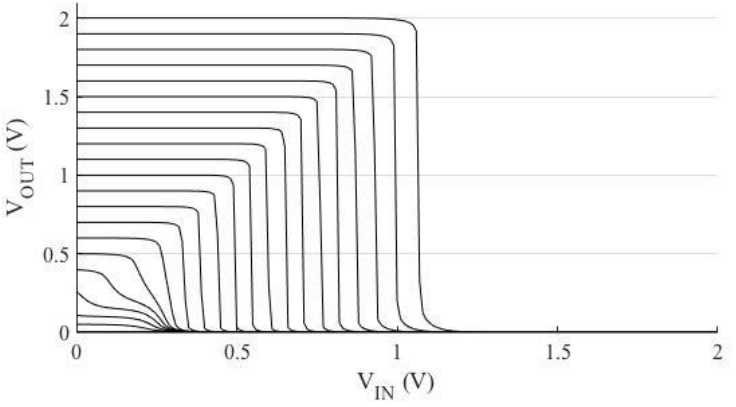


Figure 3.2. VTC of standard inverter

Figure 3.3 shows the VTC of the QFG MOS inverter for V_{DD} = 0.3 V, showing the improvement achieved with the QFG transistors. The curve is actually a transient simulation using a 10 Hz input ramp, since the QFG capacitances have no effect in DC operation.

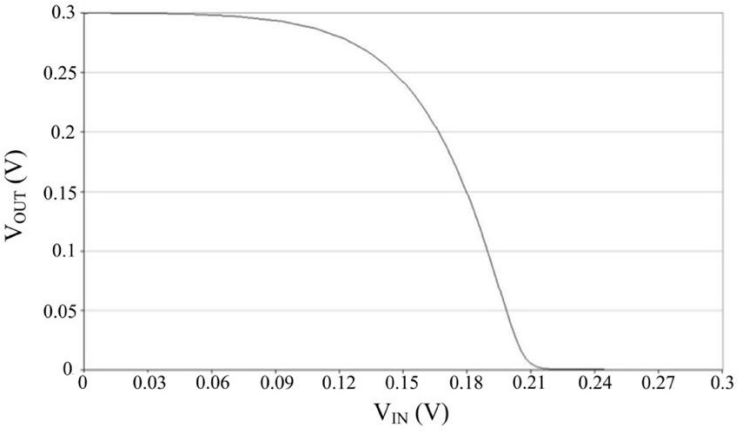


Figure 3.3. VTC of the QFG MOS inverter for V_{DD}=0.3 V

A test chip prototype including the QFG MOS inverter was fabricated and preliminary measurement results have been obtained. The coupling capacitances employed have a value of 200 fF. A microphotograph of the inverter is shown in Figure 3.4, enclosed in the white box. Silicon area employed is approximately 900 μm^2.

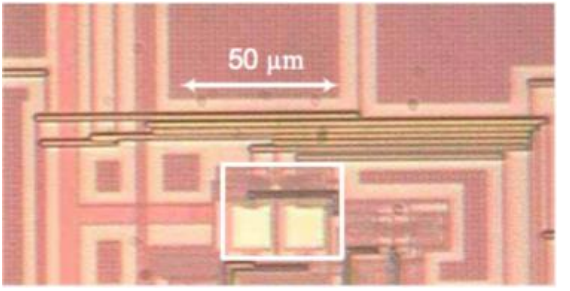


Figure 3.4. Test chip microphotograph of the QFGMOS inverter

The experimental test setup employed is shown in Figure 3.5. The Agilent 33522A signal generator is used to generate the input waveform, and the unbuffered output is directly connected to the TDS 5104 oscilloscope using a conventional test probe. Figure 3.6 shows the measured input and output

signals of the inverter, showing proper operation at a supply voltage of 450 mV. The circuit operates experimentally for supply voltages larger than approximately 300mV, much less than the threshold voltage of the technology employed. The maximum frequency of operation could not be tested due to the direct connection of the inverter to the output, which represents a load capacitance of about 30 pF including bonding pad, pin, board and probe capacitances.

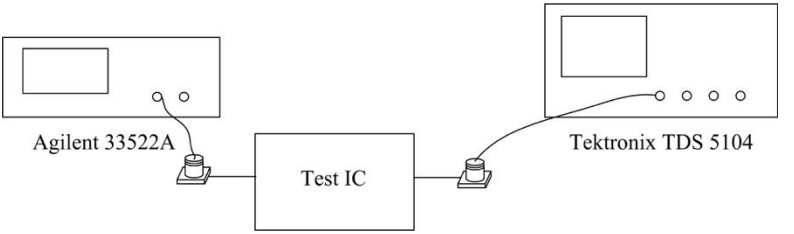


Figure 3.5. Measurement setup employed

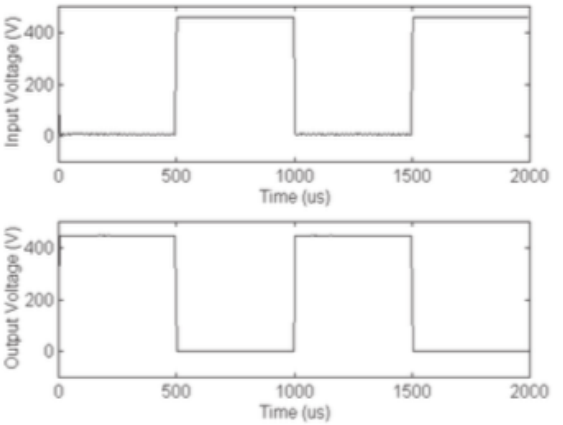


Figure 3.6. Measured input and output voltage of the QFG MOS inverter

3.2 QFG NAND, NOR and XOR gates

The procedure described above can be easily applied to other logic gates by just replacing each MOS transistor in the conventional CMOS gate by the corresponding QFG MOS version. Thus, a complete QFG MOS logic family can be generated. Figure 3.7 (a), (b) and (c) show for illustrative purposes a QFG NAND, NOR and XOR gate, respectively, obtained following this procedure.

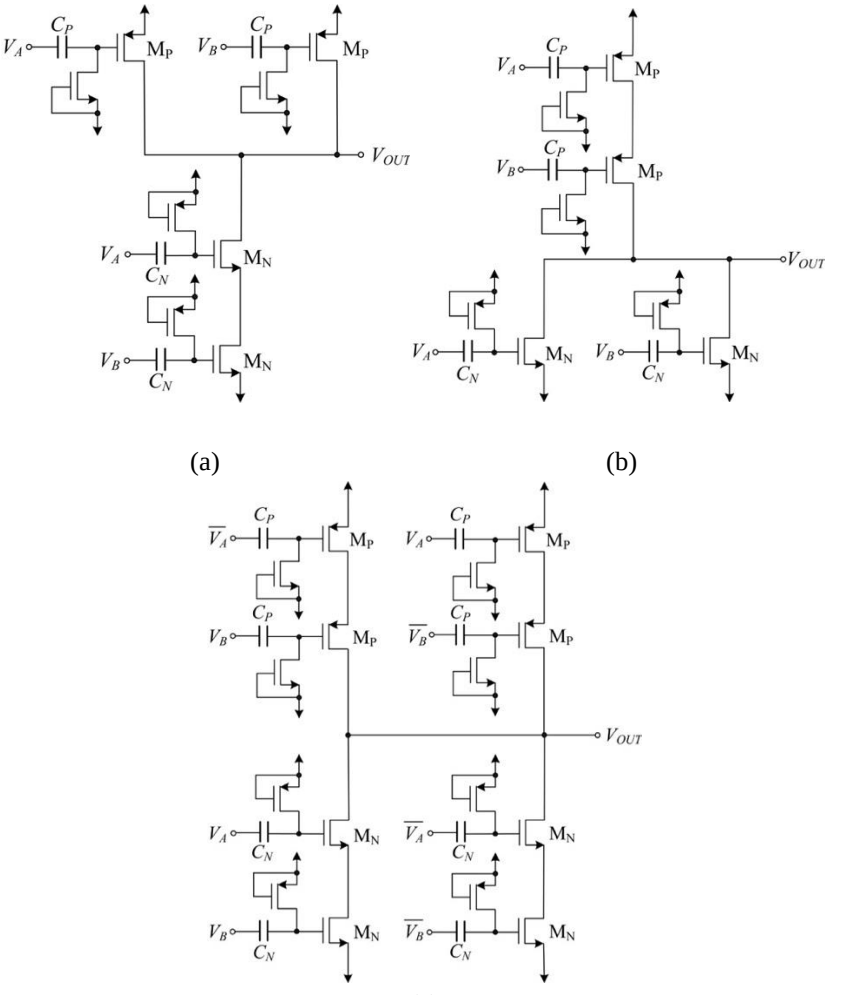


Figure 3.7. QFG Gates (a) NAND (b) NOR (c) XOR

These QFG MOS logic gates were verified only in simulation, showing also proper operation at subthreshold supply voltages.

3.3 Applications of logic gates

3.3.1 Ring Oscillator

The ring oscillator is a block that is formed by an odd number of NOT logic gates connected in series. The last inverter is connected to the input of the first NOT gate, creating a ring, hence its name. Due to the odd number of gates, there is an instability that goes from one node to the next, generating an oscillating signal in each of the nodes with different phase. Thus, it only needs a constant supply voltage V_{DD} to operate.

To evaluate the dynamic operation of the QFG MOS inverter, an 11-stage ring oscillator was designed. The topology is shown in Figure 3.8.

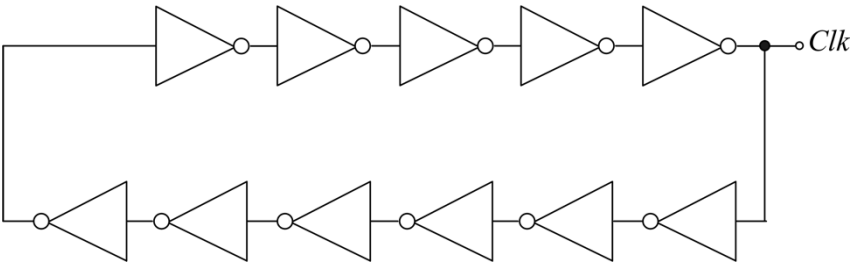


Figure 3.8. Schematic of a ring oscillator

Figure 3.9 shows the simulated voltages at the gate of the pMOS (V_{GP}) and nMOS (V_{GN}) output transistors of one of the QFG inverters of the oscillator operating with V_{DD} = 0.3 V. Note the DC level shifting of about $\pm V_{DD}/2$ theoretically predicted in the previous paragraphs.

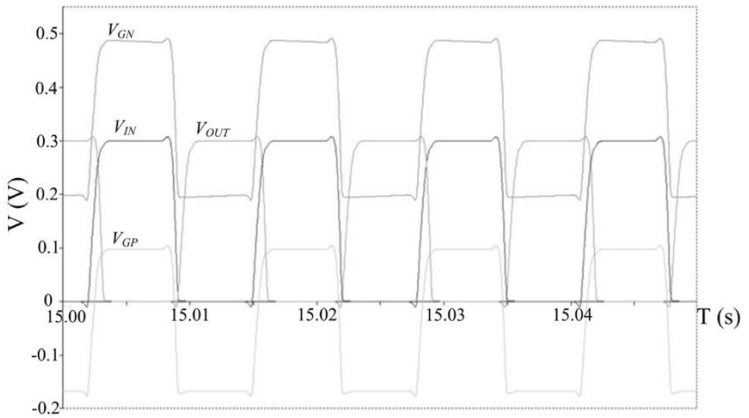


Figure 3.9. Voltage at the gates of the QFG transistors, V_{DD}=0.3V

The oscillation frequency of the oscillator versus V_{DD} is shown in Figure 3.10. The result for the oscillator implemented with the conventional CMOS inverter and a Floating Gate MOS (FGMOS) inverter [9] are also in the same figure. Note that the conventional inverter cannot operate properly below 0.4 V and that the resulting oscillation frequencies are much lower than for the QFG MOS inverter for the same V_{DD}. This is because for a given V_{DD}, the transistors in the conventional inverter deliver much less transient current than for the QFG MOS inverter due to their lower $|V_{GS}|$ voltage. The FGMOS version allows even lower V_{DD}. However, it requires complex circuits to program and refresh the charge at the floating gates, and leads to increased static power consumption.

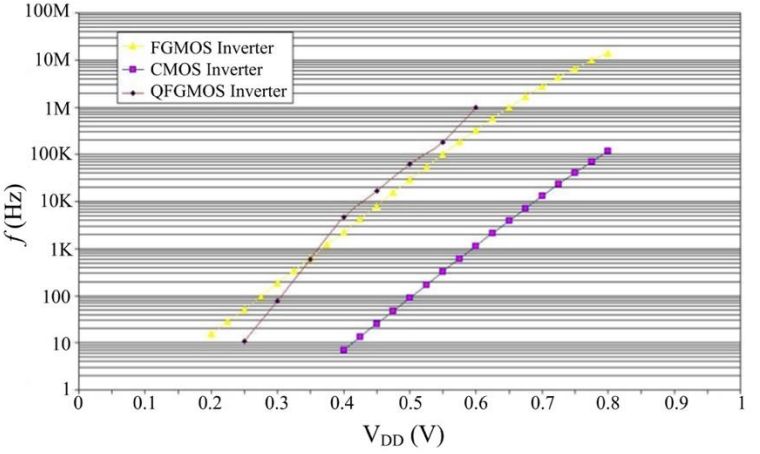


Figure 3.10. Oscillation frequency vs V_{DD}

3.3.2 Clock doubler

Clock signals are required to make synchronous logic circuits and discrete-time circuits operate. In some cases, it is convenient to use clocks whose amplitude is bigger than the supply voltage, since they are connected to the gate of transistors which behave as switches. If the amplitude of the clock is not high enough, the switches do not operate correctly, as they remain partially open or closed. To avoid this situation, boosted clocks are employed, which can be generated by a clock doubler.

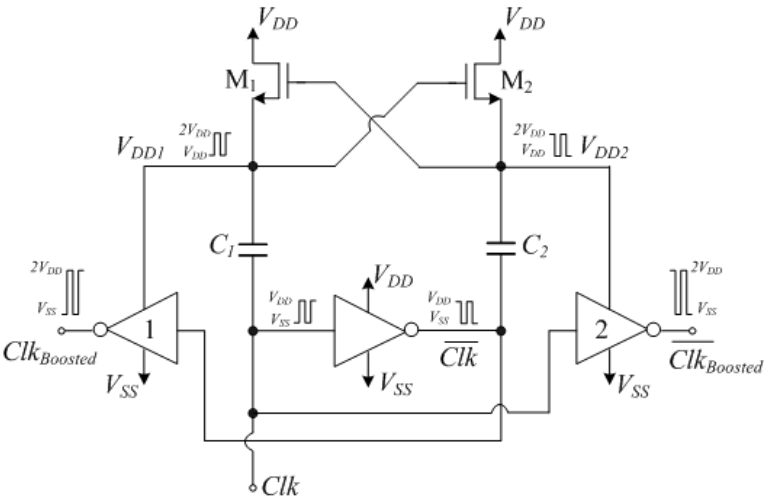


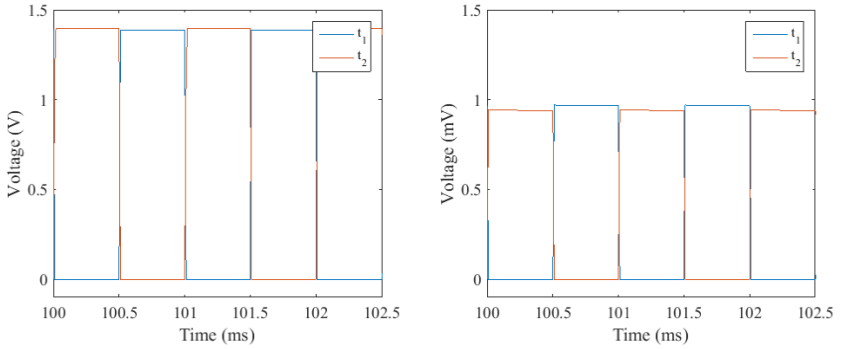
Figure 3.11. Implementation of a clock doubler

The implementation of the clock doubler can be seen in Figure 3.11 [10]. If the input clock *Clk* is V_{DD}, inverter 2 forces $\overline{Clk_{Boosted}}$ to be V_{SS}. The capacitor C_2 is charged through M_2 until it reaches a value of V_{DD}, whereas C_1 was previously charged also to V_{DD}. This makes V_{DD1} to be $2V_{DD}$, and as the input of inverter 1 is V_{SS}, the $Clk_{Boosted}$ is also $2V_{DD}$. On the contrary, when the input clock is low, V_{DD2} is $2V_{DD}$, thus $\overline{Clk_{Boosted}}$ is $2V_{DD}$. At the same time, $Clk_{Boosted}$ is V_{SS} because of the inverter 1.

The conventional clock doubler of Figure 3.11 can be improved by replacing the inverters by their QFG version, as shown in Figure 3.1. The behavior of this enhanced clock doubler is the same as the conventional one. However, due to the more convenient DC operating point, it can operate with lower supply voltage. Besides, since the output currents of the QFG inverters are greater, the clock doubler works faster.

The two versions of the clock doubler have been simulated in a 0.5 µm n-well CMOS technology. For both circuits, M_1 and M_2 have an aspect ratio of 18 µm/600 nm, 30 pF capacitors have been used as C_1 and C_2, and inverters are formed by a 18 µm/600 nm PMOS transistor and a 6 µm/600 nm NMOS transistor. In the case of QFG logic gates, C_{BAT} = 1 pF and the size of transistors M_{Rlarge} is 1.5 µm/600nm. Negative supply voltage is connected to ground in both cases, and as for the positive supply voltage, 0.7 V and 0.5 V has been used for both the conventional and QFG circuit, respectively. The input clock has a

frequency of 1 kHz, and the positive level is the same as the respective positive supply voltage. Figure 3.12 (a) and (b) present the output boosted clocks. Note that the theoretical value of the output ($2V_{DD}$) is not achieved, as there is a small voltage drop, which can be caused by the imperfect charge and discharge of the capacitors C_1 and C_2, since this process is clock-sensitive.



(a) (b)

Figure 3.12. Boosted clocks obtained with (a) conventional clock doubler (b) QFG clock doubler

3.4 Conclusions

Chapter 3 presents a subthreshold CMOS logic gate family. The use of QFG MOS transistors lead to a reduction in the supply voltage, below its threshold voltage. In addition, two possible applications of these improved logic gates have been addressed.

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Chapter 4

SINGLE-ENDED CLASS AB AMPLIFIERS

As mentioned in previous chapters, amplifiers are one of the most widely used analog building blocks, as they are required in almost every application. Most integrated amplifiers have a differential input. To realize this differential input, almost all amplifiers use what is commonly called a differential transistor pair.

If the output current is controlled by the differential input voltage, the amplifier is known as Operational Transconductance Amplifier, or OTA, being $G_m = I_{out} / V_{id}$ the transconductance gain. It can be said that OTAs are voltage controlled current sources (VCCS) with high gain.

A common method in order to increase the gain of the amplifier is using a cascode configuration, since its output resistance is higher than that of the conventional scheme. The main cascode topologies to design OTAs are depicted in Figure 4.1: (a) symmetric or current mirror OTA, (b) telescopic, (c) folded cascode and (d) recycling folded cascode. However, the symmetric topology is not going to be treated in this chapter, since many optimization efforts have already been made [1], [2]. By applying the techniques explained in Chapter 2, these different topologies are modified in this Chapter, obtaining improved performance.

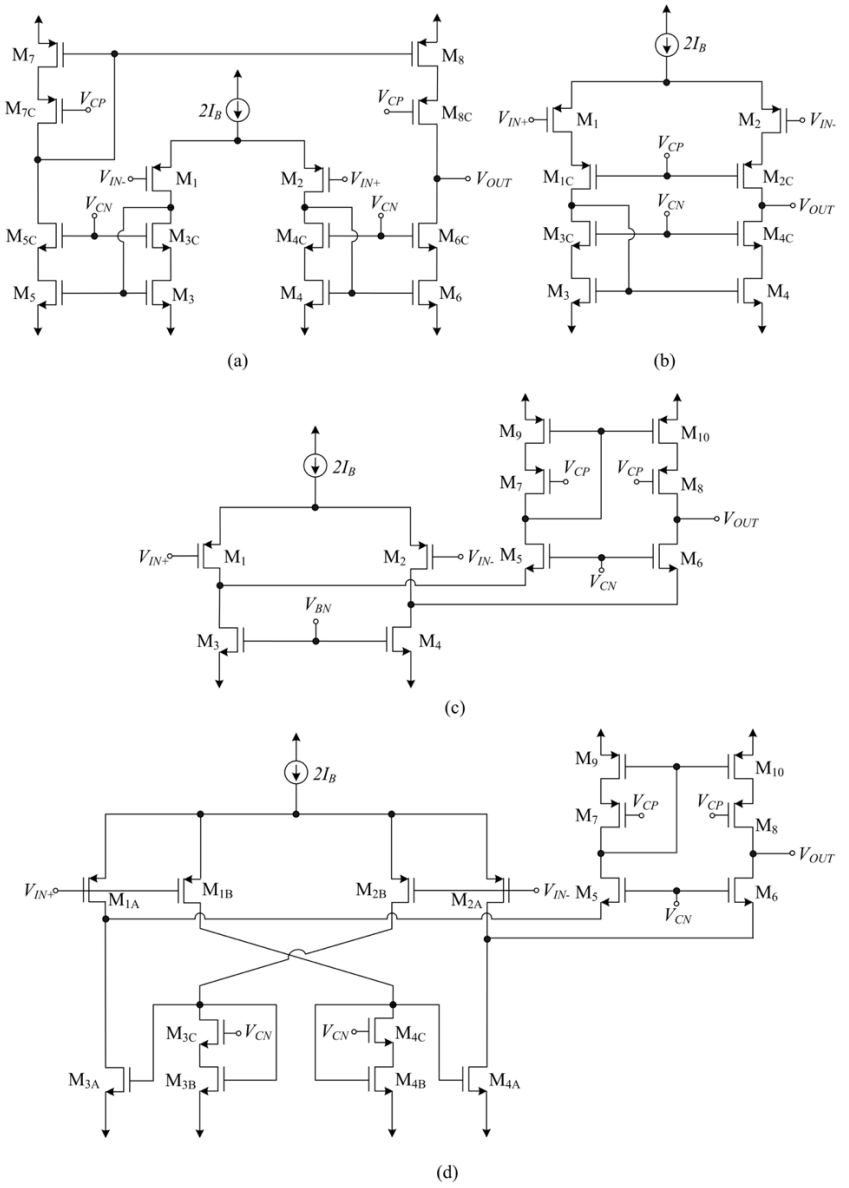

Figure 4.1. Cascode Topologies (a) Symmetric amplifier (b) Telescopic (c) Folded Cascode (d) Recycling Folded Cascode

Structure of Chapter 4 is as follows. Section 4.1 is divided in three sections, each one explaining how improved versions of the different OTA topologies can be obtained. First, an enhanced telescopic cascode OTA is proposed in Section 4.1.1. Section 4.1.2 includes a modified folded cascode OTA, and finally, several enhanced recycling folded cascode OTAs are shown in Section 4.1.3. In order to collect the main characteristics of the amplifiers proposed in Section 4.1, a table is presented in Section 4.2, including other class AB amplifiers, with the aim of comparing them. Finally, some conclusions are drawn in Section 4.3.

4.1 OTA Topologies

In this Section, several proposed OTAs are presented. They can be classified in 3 subsections, depending on which type of OTA topology they are based.

4.1.1 Telescopic Cascode

Telescopic cascode op-amps (Figure 4.2(b)) are popular since they usually provide the best trade-off between gain, power dissipation, speed, and noise. They also present optimal current efficiency $CE = I_{out}/I_{supply}$, being this parameter the ratio between the output current I_{out} to the total supply current I_{supply}. In order to obtain an optimal CE, a single branch from the supply rails to the output terminal is required, thus avoiding to waste current by extra branches replicating internally the signal currents. However, this means that input transistors must be in the output branch and therefore the input common-mode range and output swing are reduced. To mitigate these negative effects, cascode self-biasing schemes have been proposed that implement a floating battery between the common source of M_1-M_2 and the common gate of M_{1C}-M_{2C} [3]. This way, variations in the common-mode input voltage are sensed at the common source node V_S and conveyed to the gate of M_{1C}-M_{2C}, allowing low V_{DS} values for M_1-M_2 to improve output swing without degrading input common-mode range. However, such floating battery has been often implemented by a diode-connected transistor (or less frequently by a resistor) biased by two matched DC current sources, which increases static power consumption and matching requirements.

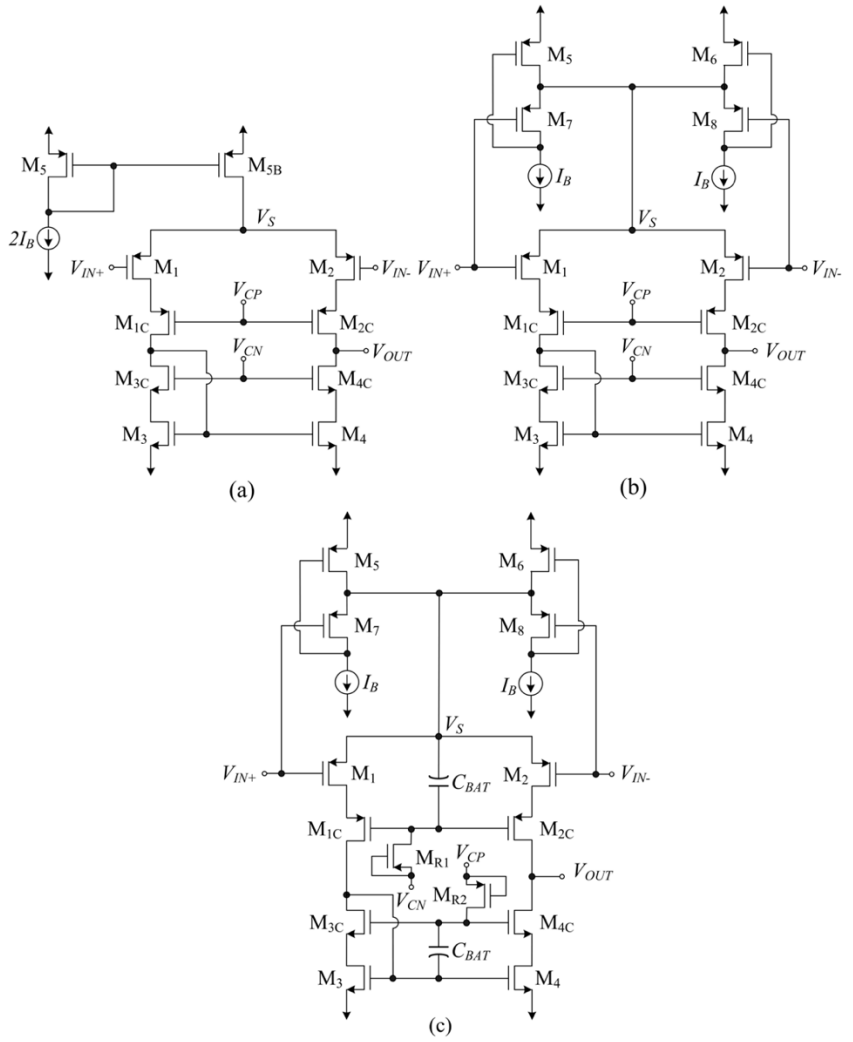

Figure 4.2. Telescopic OTAs (a) Conventional (b) Class AB (c) Proposed QFG Class AB

Another drawback of the opamp of Figure 4.2(a) is that it operates in class A, delivering a maximum output current limited by the bias current. Hence a trade-off between static power dissipation and dynamic performance exists. An adaptive bias current source can be used instead to get class AB operation. However, in this case although self-biasing was used in the PMOS cascode transistors, the large dynamic currents generated can make transistors M_3-M_4

leave saturation, reducing slew rate (SR). Hence dynamic biasing is also required for the NMOS cascode transistors.

A class AB single-stage telescopic cascode opamp is proposed. It employs an adaptive bias current source and a dynamic biasing technique for the cascode transistors which does not lead to extra power consumption or matching requirements.

Figure 4.2(b) shows the telescopic cascode opamp with the adaptive bias circuit employed. Transistors M_5, M_6, M_7 and M_8 and bias current sources I_{BIAS} implement a maximum circuit [4] that sets voltage $V_S = max(V_{IN+}, V_{IN-})+V_B$, where DC voltage V_B is the quiescent V_{SG} voltage of M_7-M_8. In quiescent operation $V_{SG1,2}=V_B$, so quiescent current in M_1-M_2 is accurately set to I_{BIAS}/n with $n = (W/L)_{7,8} / (W/L)_{1,2}$ regardless of process, supply voltage or temperature variations. When $V_{IN-} < V_{IN+}$, M_7 enters triode region and V_S is set to $V_{IN+} + V_B$, so $V_{SG1} = V_B + V_{IN+} - V_{IN-}$, i.e., M_1 experiences the full input signal swing and a large dynamic current not bounded by I_{BIAS} is generated at M_1. Analogously, when $V_{IN-} > V_{IN+}$ then $V_S = V_{IN+} + V_B$ and a large dynamic current is created in M_2. However, in small signal operation the common source node is a small-signal ground, so AC small signal currents in M_1-M_2 are like in Figure 4.2(a) and gain-bandwidth product (GBW) is not improved by the adaptive biasing.

Despite the large dynamic current that can potentially be generated, the circuit of Figure 4.2(b) is not efficient since the static biasing at the cascode transistors can make M_1 and/or M_3-M_4 enter triode region for $V_{IN-} < V_{IN+}$ or can turn M_2 in triode mode for $V_{IN-} > V_{IN+}$. To solve it, cascode transistors are dynamically biased using Quasi-Floating Gate (QFG) techniques [5] as shown in Figure 4.2(c). As described in Section 2.1.2, minimum-size transistors M_{R1} and M_{R2} are pseudo resistors with very large resistance R_{large}. Hence capacitors C_{BAT} cannot discharge rapidly and behave as floating DC level shifters, transferring signal variations from the common source of M_1-M_2 to the gate of M_{1C}-M_{2C} and from the gate of M_3-M_4 to the gate of M_{3C}-M_{4C}. In quiescent state capacitors C_{BAT} are open circuits and the op-amp is equivalent to Figure 4.2(b). However, in dynamic operation the cascode biasing allows handling large signal currents. Note that no extra power consumption or matching requirements are needed for the dynamic biasing employed. Moreover, due to the extremely large R_{large} values achieved, $C_{BAT} < 1$ pF can be employed, reducing the silicon area overhead.

Concerning small signal operation, the DC gain A_d and GBW of the three opamps of Figure 4.2 are the same:

$$A_d = g_{m1,2} \cdot R_{out} \approx g_{m1,2} \cdot (g_{m2c} \cdot r_{o2c} \cdot r_{o2} \parallel g_{m4c} \cdot r_{o4c} \cdot r_{o4}) \quad (4.1)$$

$$\text{GBW} = g_{m1,2}/(2\pi C_L) \quad (4.2)$$

with g_{mi} and r_{oi} are the transconductance and output resistance, respectively, of transistor M_i. However, CMRR is improved in Figure 4.2(c) as the dynamic cascode biasing tracks input common-mode variations from the common source node V_S to the gate of M_{1C}-M_{2C}, keeping the V_{DS} of M_1-M_2 almost constant.

A test chip prototype with the amplifiers of Figure 4.2 was fabricated in a 0.5 µm CMOS process. Poly-poly capacitors C_{BAT} were used with a nominal value of 850 fF. Transistor aspect ratios are shown in Table 4.1. A microphotograph of the three amplifiers is shown in Figure 4.3, where their relative areas can be assessed.

Transistor	**W/L** (µm/µm)
M_1, M_2	100/1.05
M_3, M_4	120/0.6
M_{1C}, M_{2C}, M_3, M_4	200/0.6
M_5, M_{5B}, M_6	100/0.6
M_7, M_8	100/1.05
M_{R1}, M_{R2}	1.5/1.05

Table 4.1. Transistors aspect ratios of telescopic OTA in Figure 4.2

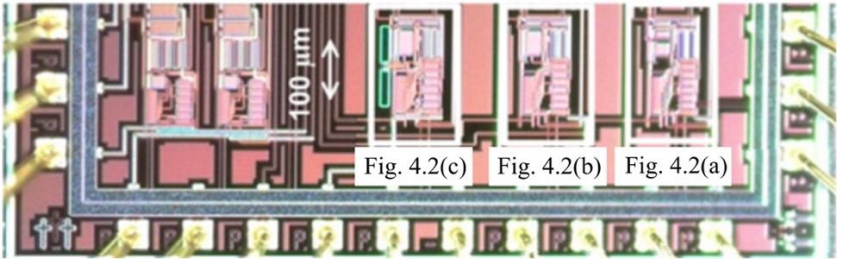

Figure 4.3. Microphotograph of the three telescopic OTAs

Measurements were done using the amplifiers in unity-gain negative feedback as voltage followers. Supply voltage was ±1 V. No external load capacitance was used, so C_L corresponds to the capacitance of the test setup (pad, board and test probe) and is approximately 20 pF. The measured transient response of the three amplifiers is shown in Figure 4.4. The class A amplifier corresponds to Figure 4.2(a), Class AB to Figure 4.2(b) and the proposed one to Figure 4.2(c). A 100 kHz 1 V input square wave was used. Note the improved SR and output swing achieved with the circuit of Figure 4.2(c).

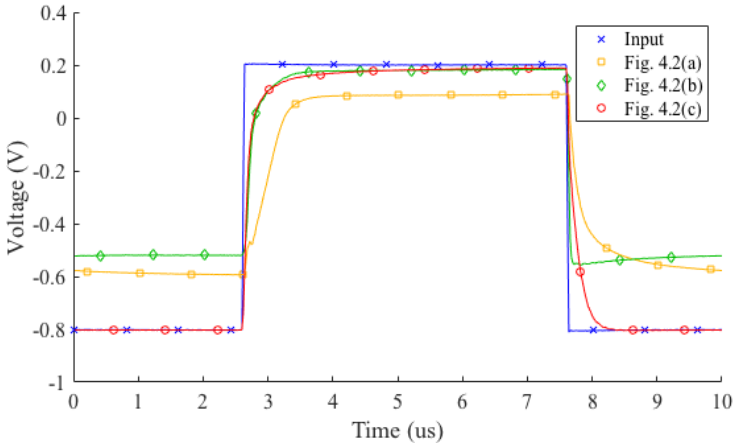

Figure 4.4. Measured transient response of the circuits of Figure 4.2

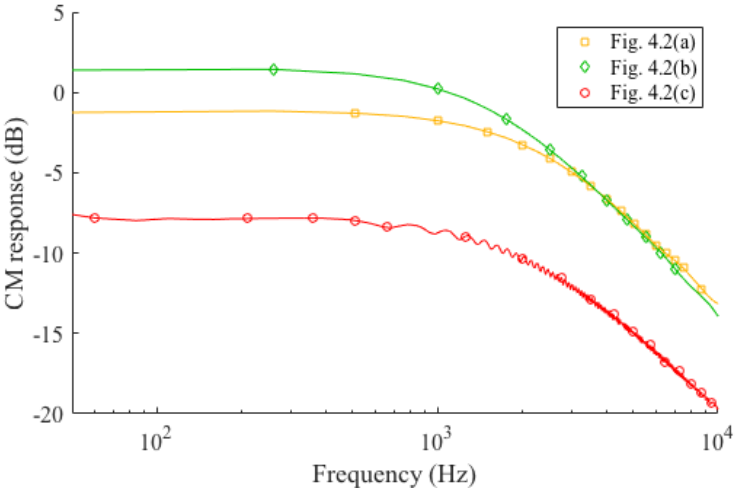

Figure 4.5. Measured magnitude response of the A_{cm} of circuits of Figure 4.2

The measured magnitude response of the common-mode gain $A_{cm}=v_{out}/v_{icm}$ is shown in Figure 4.5. Higher A_{cm} (hence lower CMRR=A_d/A_{cm}) in Figure 4.2(b) vs Figure 4.2(a) is due to the smaller output resistance of the adaptively biased current source M_5-M_8 vs the current source M_{5B} in Figure 4.2(a). However, the dynamic cascode biasing in Figure 4.2(c) improves noticeably A_{cm} and hence CMRR, as mentioned above.

Table 4.2 summarizes the main performance parameters of the opamps of Figure 4.2. The measured THD for Figure 4.2(c) is higher due to the improved signal swing and SR achieved. A comparison with other micropower class AB amplifiers is shown in Figure 4.6, using the figure of merit FoM = $SR \cdot C_L/I_{supply} = I_{maxI}/I_{supply}$, where I_{supply} is the total static current consumption. Note the improved FoM vs power data achieved for the proposed opamp of Figure 4.2(c).

Parameter	Figure 4.2(a)	Figure 4.2(b)	Figure 4.2(c)
Slew Rate	1 V/μs	5.3 V/μs	8.9 V/μs
THD @100kHz, 0.7V_{pp}	-18.1 dB	-14.1 dB	-41.9 dB
DC gain (*)	54.1 dB	54.6 dB	54.6 dB
PM (*)	88.7º	88.4º	88.4º
GBW (*)	1.15 MHz	1.15 MHz	1.15 MHz
CMRR	55.3 dB	53.2 dB	62.4 dB
PSRR+	85.1 dB	73.6 dB	77.6 dB
PSRR-	68.9 dB	65.8dB	67.3 dB
Eq. input noise @1MHz (*)	22 nV/√Hz	23 nV/√Hz	23 nV/√Hz
Power	80 μW	80 μW	80 μW
Area	0.019 mm^2	0.020 mm^2	0.023 mm^2

(*)Simulation

Table 4.2. Measured performance summary and comparison between op-amps of Figure 4.2 (C_L = 20 pF)

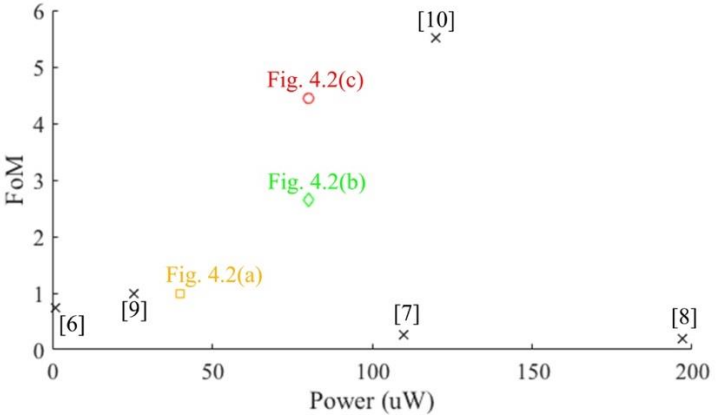

Figure 4.6. Performance comparison between other op-amps

To sum up this section, a micropower telescopic opamp has been proposed. It employs various adaptive biasing techniques for providing bias currents and cascode bias voltages. These techniques improve dynamic operation maintaining supply voltage requirements and quiescent currents, without degrading other performance metrics.

4.1.2 Folded Cascode

As it was mentioned in Chapter 2, class AB amplifiers are widely used in applications requiring low power consumption due to their capacity to yield large dynamic currents not limited by the quiescent currents. Thus, low static power consumption can be obtained without degrading dynamic performance. An adaptive bias circuit for the differential pair is usually employed to get the required current boosting, providing very low quiescent currents in order to have very low static power dissipation. However, when a large differential input signal is applied, these adaptive bias circuits are able to provide large dynamic currents, with maximum swings larger than the quiescent current level.

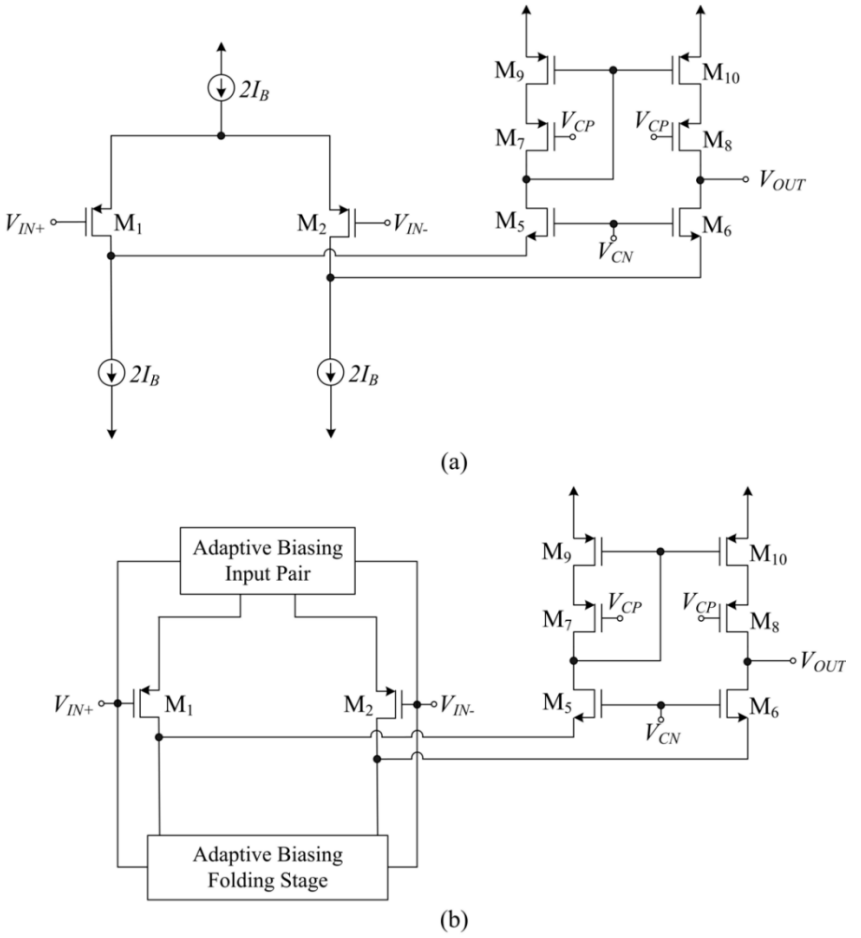

Figure 4.7. Folded Cascode (a) Conventional Class A OTA (b) Proposed Class AB OTA

Several proposals have been reported to provide class AB operation to classic amplifier topologies like telescopic and current mirror OTAs, e.g. [1], [6], [11]. However, achieving class AB operation in a folded cascode amplifier (Figure 4.7(a)) is more complex. Adaptive biasing of the input pair is not effective by itself in this case since the bottom current sources limit the maximum output current. As these current sources force the sum of currents through M_1 and M_5 to be $2I_{BIAS}$, and the same with the sum of currents through M_2 and M_6, the maximum output current is $2I_{BIAS}$ regardless of the adaptive biasing circuit used for the input pair. Therefore, it is mandatory that these bias

current sources also adapt to the input signal to achieve power efficiency. Thus, multi-path schemes [12], [13] or current recycling techniques [14]-[17] are usually employed to enhance the performance of the folded cascode amplifier, replacing these current sources by active current mirrors. However, the power efficiency achieved with these techniques is limited since the active current mirrors lead to internal replication of large dynamic currents at the additional branches [1]. A simple modification of the conventional folded cascode OTA is proposed which enhances the performance of the amplifier without this drawback.

Figure 4.7 (a) and (b) shows the conventional class A folded cascode OTA and the proposed class AB OTA, respectively. The constant differential pair bias source $2I_B$ of Figure 4.7(a) is replaced in Figure 4.7(b) by an adaptive circuit to bias M_1 and M_2. Besides, the current sources $2I_B$ at the folding stage of conventional OTA are replaced by another adaptive biasing circuit in the proposed OTA, so that the limitation in output current is avoided.

In order to implement the adaptive biasing circuit of the input pair, cross-coupled floating batteries are used (previously explained in Section 2.2.3.1) [1],[18]. The employed topology is shown in Figure 2.20. This way, thanks to two Flipped Voltage Followers (FVFs) [19], in quiescent conditions, accurate low quiescent currents are provided and in dynamic conditions, large currents are achieved, not bounded by $2I_B$. In addition, the full differential input signal is applied to each differential pair transistor, thus doubling DC gain compared to class A OTA.

However, although the adaptive biasing circuit of the input stage would double DC gain (and GBW), it could not increase dynamic output currents, as currents in the output branches are limited by the current sources of the folding stage. To overcome this issue, here current sources are also adaptively biased, this time by using Quasi-Floating Gate transistors [20], [21]. The concept of using QFGMOS transistors to achieve class AB operation was previously described in Section 2.1.2 (see Figure 2.6). Thus, an efficient implementation of a DC level shifter is obtained only with a capacitor and a high value resistance. The quiescent current through M_3 and M_4 is still $2I_B$ but under dynamic conditions, voltages at the gates of M_3 and M_4 experience a swing dependent on V_{IN}, creating an extra signal path.

The schematic of the proposed Class AB folded cascode OTA is shown in Figure 4.8. Note that the QFG transistors M_3 and M_4 are not directly connected to the input signal. They re-use the FVFs to invert and scale the input signals to fit the signal swing at the gates of M_3 and M_4 and to avoid extra loading of the input terminals by the adaptive biasing of the folding stage.

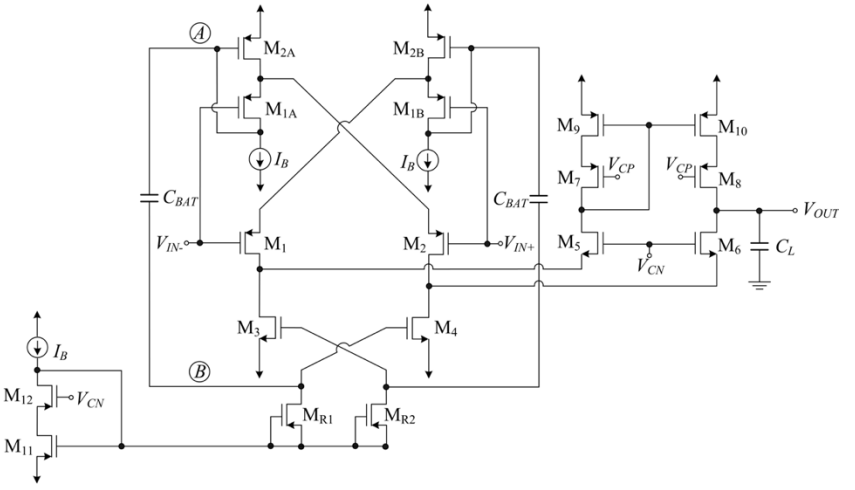

Figure 4.8. Proposed class AB folded cascode OTA

In quiescent operation, the proposed circuit works like the conventional OTA in Figure 4.7(a), with well controlled quiescent currents, as there is no current flowing through the pseudo resistors M_{R1} and M_{R2}. For large positive differential input voltages, $V_{ID} = V_{IN+} - V_{IN-}$, the gate voltage of M_{2B} decreases and that of M_{2A} increases. As it was mentioned in Chapter 2, capacitors C_{BAT} act as floating batteries that decrease the gate voltage of M_4 and increase that of M_3. Thus, a large output current is sourced to the load, yielding large positive Slew Rate SR_+. For negative V_{ID}, something similar happens. The gate voltage of M_{2B} increases and that of M_{2A} decreases, increasing the gate voltage of M_4 and decreasing that of M_3, leading to a large output current sunk from the load that boosts SR_-.

If small-signal analysis is considered, the adaptive biasing employed in Figure 4.8 not only increases slew rate, it also significantly increases the transconductance G_m of the conventional OTA for the same bias current and transistor sizes. The transconductance of the conventional folded cascade OTA is defined by:

$$G_{mA} = g_{m1} = g_{m2} \tag{4.3}$$

while that of the proposed OTA in Figure 4.8 is:

$$G_{mAB} = 2g_{m1}\left(1 + \alpha \frac{g_{m3,4}}{g_{m2A,2B}}\right) \tag{4.4}$$

with $\alpha \approx C_{BAT}/(C_{BAT} + C_{gs3,4})$. Thus, the increase factor is $2\cdot(1+\alpha\cdot g_{m3,4}/g_{m2A,2B})$. The factor 2 is caused by the adaptive biasing circuit of the differential pair and the term $1+\alpha\cdot g_{m3,4}/g_{m2A,2B}$ corresponds to the adaptive current sources M_3 and M_4. The same enhancement factor is present in the GBW of the proposed class AB OTA compared to the conventional class A OTA. The DC gain of the class AB OTA is also increased, but to a less extent since the output resistance R_{out} of the class AB OTA is also slightly decreased due to the nonzero output resistance of the FVFs.

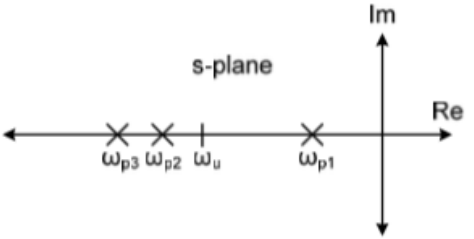

Figure 4.9. Simplified pole-zero diagram (not to scale)

Just like the conventional folded cascade OTA, the proposed OTA features a dominant pole $\omega_{p1} = -1/(R_{out}\cdot C_{out})$ set by the output terminal as well as a non-dominant pole $\omega_{p3} \approx -g_{m5,6}/C_{p5,6}$ corresponding to the source terminals of M_5 and M_6. In these expressions $C_{out} \approx C_L$ is the output capacitance and $C_{p5,6}$ is the parasitic capacitance at the source of M_5 and M_6, which corresponds to $C_{gs5,6}$ plus other smaller capacitances. In addition, the circuit in Figure 4.8 has an additional non-dominant pole $\omega_{p2} \approx -g_{m2A,2B}/(C_A + \alpha\cdot C_B)$, due to the extra signal path introduced, where C_A and C_B are the parasitic capacitances at nodes *A* and *B*, respectively. C_A is approximately $C_{gs2A,2B}$ plus the bottom plate to the substrate parasitic capacitance of C_{BAT}, and C_B is approximately $C_{gs3,4}$ plus the top plate to substrate parasitic capacitance of C_{BAT}. All these poles are depicted in Figure 4.9, where it is assumed that non-dominant poles are beyond the unity-gain frequency ω_u. Since ω_{p2} is associated to PMOS devices, and $C_A + \alpha\cdot C_B$ is generally larger than $C_{p3,4}$, ω_{p2} is at lower frequencies than ω_{p3}. Hence ω_{p2} yields a reduction in phase margin compared to the class A version.

For this additional pole frequency to be at least 3 times the GBW, the required C_L is approximately

$$C_L > 6\frac{g_{m1,2}}{g_{m2A,2B}}\left(1+\alpha\frac{g_{m3,4}}{g_{m2A,2B}}\right)\cdot(C_A+\alpha C_B) \tag{4.5}$$

As for the slew rate, that of the conventional folded cascode in Figure 4.7(a) is

$$SR_{A+} = SR_{A-} = \frac{2I_B}{C_L} \tag{4.6}$$

since $2I_B$ is the maximum current sourced to the load of sunk from it. Thus, symmetrical positive and negative slew is provided but the maximum output current is limited by the bias current. In the case of proposed folded cascode OTA, the expression for the slew rate is

$$SR_{AB+} = SR_{AB-} = \frac{2I_B}{C_L}\left(1+\alpha\sqrt{\frac{\beta_{3,4}}{\beta_{2A,2B}}}\right) \tag{4.7}$$

with $\beta_i = \mu \cdot C_{ox}(W/L)_i$, evidencing the SR improvement achieved.

Both the class A and class AB folded cascode OTA circuits of Figure 4.7(a) and Figure 4.8 were fabricated in a 0.5 μm CMOS test chip prototype. A microphotograph of that chip is shown in Figure 4.10, where the OTAs are enclosed by white rectangles. The transistor sizes employed are included in Table 4.3. Poly-poly capacitors C_{BAT} were used, with a value of 0.7 pF. Supply voltages where ±1 V, and the bias current I_B was 10 μA. Cascode bias voltages V_{CP} and V_{CN} were set to -0.2 V and 0 V, respectively. An external load capacitor of 47 pF was used. The output was connected directly to a bonding pad and no external buffer was employed. Thus, if the pad, board and test probe capacitances are considered, the total load capacitance is increased to approximately 70 pF.

Figure 4.10. Test chip microphotograph

Transistor	**W/L** (μm/μm)
M_1-M_2, M_{1A}-M_{1B}	100/1.5
M_{2A}-M_{2B}	9/0.6
M_3-M_4	120/0.6
M_5-M_8	200/0.6
M_9-M_{10}	200/1.05
M_{11}	60/0.6
M_{12}	100/0.6
M_{R1}-M_{R2}	1.5/0.6

Table 4.3. Transistor aspect ratio of class AB folded cascode OTA

The transient response of both fabricated OTAs was measured in unity gain configuration, using a 1 MHz 0.5 V square wave with DC level of -0.6 V at the input. The measured output of both OTAs are drawn in Figure 4.11. Note the stable and faster settling of the proposed class AB OTA of Figure 4.8. The SR_+ for the class A OTA is 0.32 V/μs and that of the proposed class AB OTA is 9.8 V/μs, i.e., an increase factor of 30.6 for the same quiescent current and load capacitance. The expected increase factor from Equation 4.7, with estimated $\alpha \approx 0.8$, was 36.

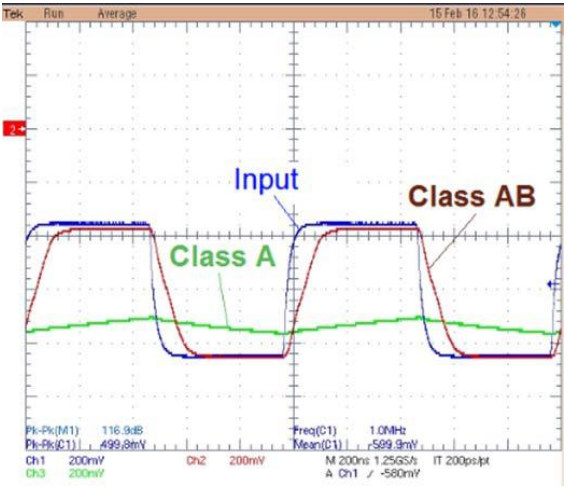

Figure 4.11. Measured response of class A and class AB folded cascode OTAs

As can be noticed from Equation 4.5, the OTA is suitable for relatively large C_L. To solve this limitation, lead compensation at the output terminal is proposed, as shown in Figure 4.12. By using this method, lower C_L values can be employed.

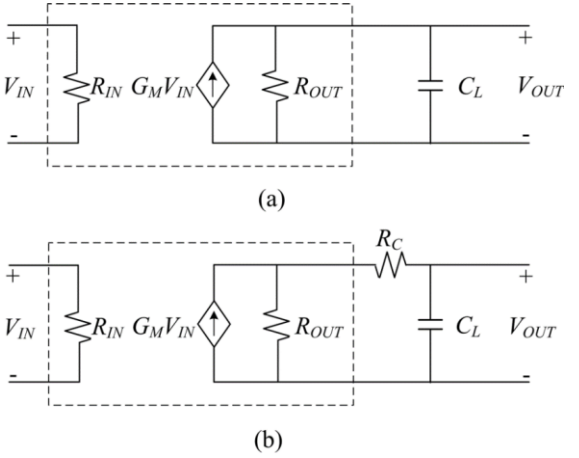

Figure 4.12. Simplified AC model (a) Purely capacitive load (b) with lead compensation

To analyze the effect of the added resistor R_C, the basic single-pole AC model of the FC OTA will be used for simplicity. The transfer function of Figure 4.12(a) is

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G_m R_{out}}{1+sR_{out}C_L} \tag{4.8}$$

If a resistor R_C is placed in series with the capacitive load, as Figure 4.12(b) shows, the transfer function becomes

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G_m R_{out}(1+sR_C C_L)}{1+s(R_{out}+R_C)C_L} \tag{4.9}$$

Thus, the lead compensation resistance R_C creates a zero $\omega_z \approx -1/(R_C \cdot C_L)$ that can be placed at different locations to improve phase margin and settling performance [22]. The strategy followed here is to choose R_C in order to make ω_z slightly larger than the unity-gain frequency, leading to a phase lead equal to $arctan(\omega_z/GBW)$ rads in the phase margin. In addition, it can be deduced from expression 4.9 that the output pole is modified by R_C, but if $R_C << R_{out}$, this variation can be neglected.

The schematic of the proposed folded cascode OTA with lead compensation is presented in the figure below.

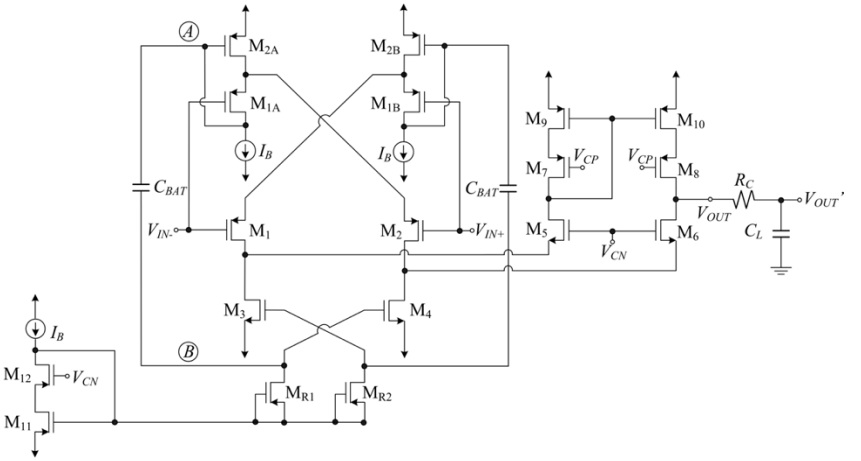

Figure 4.13. Enhanced folded cascode with lead compensation

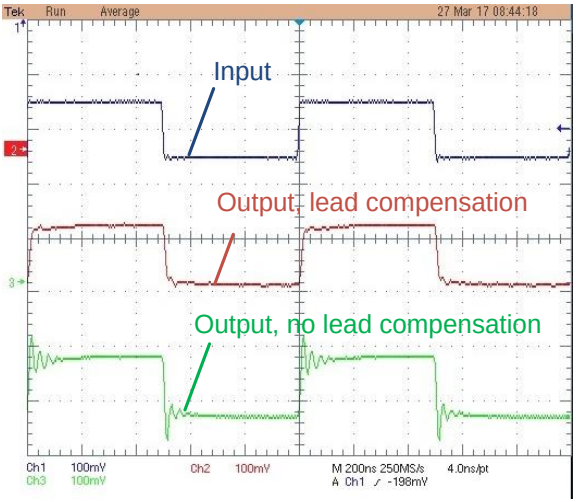

Figure 4.14. Measured transient response without external C_L

To assess the improvement provided by the lead compensation, Figure 4.14 shows the transient response of the proposed OTA with no external load capacitor, i.e. the load capacitance is only that of the test setup, whose estimated value is of approximately 23 pF. The input signal applied is a 1 MHz 100 mV periodic square waveform with DC level of -200 mV. Note that there

is a significant ringing in the output waveform when no lead compensation is employed, which degrades settling performance. The inclusion of a lead resistance R_c of 772 Ω improves settling performance significantly, as the red curve shows.

The measured magnitude response of the class A and class AB OTAs as voltage followers is shown in Figure 4.15. The cutoff frequency of the proposed OTA is 4.75 MHz, while that of the conventional OTA is 310 kHz. Due to the dominant pole design, these frequencies correspond approximately to the GBW of the OTAs. Thus, the experimental increase factor in GBW is 15.3. The expected value from Equation 4.4 with $\alpha \approx 0.8$ was 12.2.

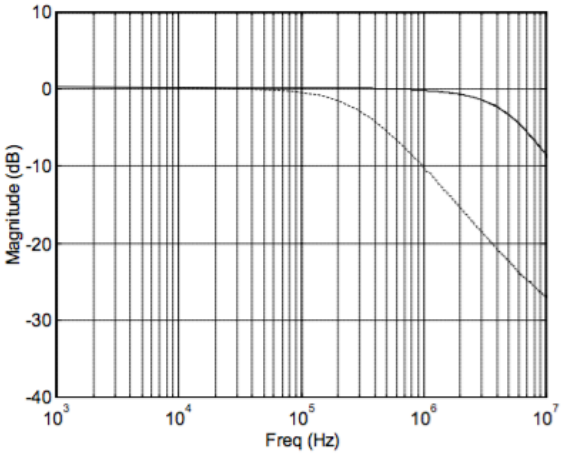

Figure 4.15. Measured closed-loop magnitude response of conventional class A OTA (dashed line) and proposed class AB OTA (solid line)

Table 4.8 sums up the main measurement results for both OTAs. Note that the settling time in the proposed OTA is lower than 100 ns, whereas the conventional OTA is unable to settle for this input signal and load. Measured Total Harmonic Distortion (THD) is <1% for a 1 V_{pp} input sinusoidal signal, while the conventional OTA presents a THD >6% due to settling limitations. The open-loop frequency response could not be measured because of the high gain. Simulation results for DC gain and phase margin are provided instead. The increase in DC gain of the proposed OTA is 14.6 dB (i.e. a factor of 5.37), lower than the GBW increase factor due to the reduced output resistance. These results agree with theoretical analysis. The main disadvantage of the proposed OTA is

the decrease in phase margin. The PM of the conventional OTA drops to 79º at 4.75 MHz, so the proposed OTA shows a degradation of 19º.

The proposed OTA presents a slightly lower equivalent input noise level, due to the increased gain. However, there is a 50% increase in the static power because of the bias current required for the FVFs. Besides, silicon area is a 20% higher due to capacitors C_{BAT}. If the width of M_{1A} and M_{1B} is reduced by a factor n than that of M_1 and M_2, the bias current of the FVF is also scaled by n, and the extra required power would be $50/n$ %.

A performance comparison with other proposed class AB amplifiers is also included in Table 4.8. To ease comparison, two conventional Figures of Merit (FoM) are considered: $FoM_L = SR \cdot C_L/I_{supply} = I_{maxL}/I_{supply}$, where I_{supply} is the total current consumption, which shows the large-signal current efficiency, and $FoM_S = 100 \cdot GBW \cdot C_L/I_{supply}$ (MHz·pF/μA) a small-signal speed/power ratio. Note that the proposed OTA compares favorably for both FoMs.

As a conclusion, a class AB folded cascode OTA has been presented, based on two adaptive biasing circuits for the differential input pair and the folding stage. The use of FVFs and QFG transistors leads to a simple and compact implementation and does not require extra supply voltage. Measurement results show a significant increase in slew rate and fast settling, maintaining low noise and low static power consumption. The circuit can find application in low voltage low power switched capacitor circuits and in buffers requiring to drive large capacitive load.

4.1.3 Recycling Folded Cascode

In the previous section, an improved version of the conventional folded cascode OTA was discussed. Although its transconductance was improved thanks to the use of QFG transistors at the folding stage, dynamic performance can be further improved.

A highly power-efficient approach to achieve class AB amplifiers was proposed in [1]. Although it employs the same adaptive biasing technique for the differential pair as the previous class AB folded cascode OTA, its output currents are ideally proportional to V_{id}^4, where V_{id} is the differential input voltage, thus achieving greater output current values. Since dynamic currents in conventional class AB differential amplifiers are often proportional to V_{id}^2, the

OTAs proposed in [1] were coined as “super” class AB OTAs. Besides very large SR, the most salient feature of super class AB OTAs is that they exhibit high power efficiency since they are single stage topologies where large dynamic currents are generated directly at the output transistors, without internal replication (apart from the unavoidable replication at the output current mirror load for single-ended outputs). However, super class AB techniques (and hence their inherent advantages) have been restricted so far to the current mirror OTA architecture. In this thesis, these techniques are applied to the RFC OTA, thus combining the benefits of both approaches.

The conventional (class A) PMOS-input folded cascode OTA is shown in Figure 4.16(a). Note that the differential pair transistors M_1-M_2 have been split into two identical transistors (M_{1A}-M_{1B} and M_{2A}-M_{2B}). The same has been done with the current sources M_3 and M_4 at the folding stage (split into M_{3A}-M_{3B} and M_{4A}-M_{4B}). This has been done just to ease comparison with the other topologies described in this section. The differential pair bias current source $2I_B$ provides a quiescent current $I_B/2$ to M_{1A}, M_{1B}, M_{2A} and M_{2B}. If each pair of current sources at the folding stage (M_{3A}-M_{3B} and M_{4A}-M_{4B}) provides a DC current $2I_B$, then the remaining transistors M_5 to M_{10} are biased with a current I_B.

Figure 4.16(b) shows the PMOS-input RFC OTA [14]. It is designed by replacing the current sources at the folding stage by active current mirrors with current ratio 1:K, and reconnecting the differential pair transistors. Note that if factor K=3, power consumption is the same as for the FC OTA of Figure 4.16(a). Transistors M_{3C}-M_{4C} are included to improve accuracy of the current mirrors. This arrangement increases the transconductance, GBW and SR of the OTA without the need to increase current consumption, since folding is made by active current mirrors with current gain K which scale the signal currents generated by the differential pair. The conventional FC OTA requires a large DC current just to invert (fold) the differential pair signal current, without providing current gain and thus wasting static power. Note also that the RFC OTA can be regarded as a three-current mirror OTA with an additional signal path formed by the extra differential pair M_{1A} and M_{2A} cross-connected to the folding nodes at the output branch.

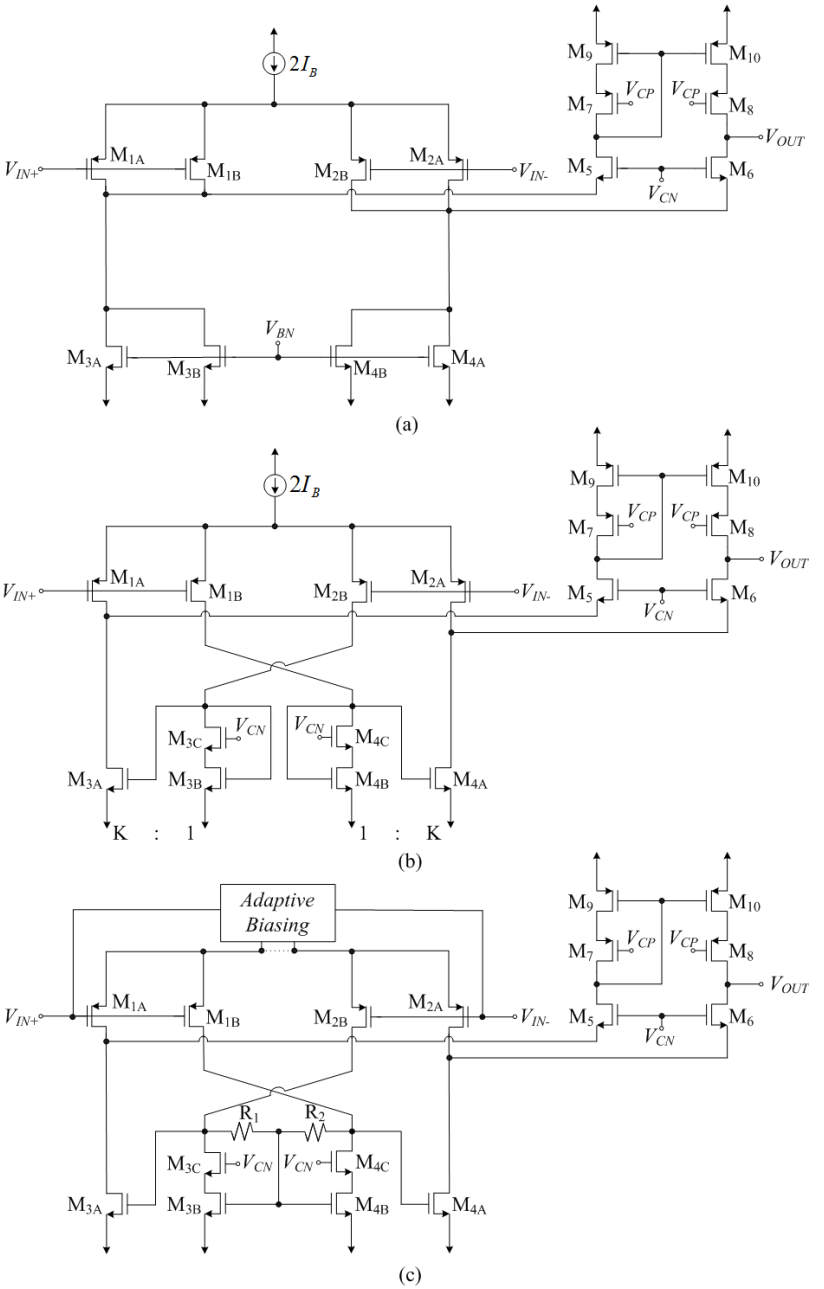

Figure 4.16. (a) Folded Cascode OTA (b) Recycling Folded Cascode OTA (c) Super Class AB Recycling Folded Cascode OTA

Despite the advantages of the RFC OTA, its power efficiency is limited, due to two main reasons: First, the current gain K scales both dynamic and static currents. Hence, although SR is K times higher than for the FC OTA it is still proportional to I_B and thus proportional to static power consumption. Second, the active current mirrors included lead to internal copy of dynamic currents, degrading current efficiency [1].

Figure 4.16(c) shows a power-efficient super class AB implementation of the RFC OTA proposed here, which solves these shortcomings. An adaptive bias circuit replaces the constant current source $2I_B$ that bias the differential pair. This way, low static currents can be set and at the same time dynamic currents not limited by I_B can be generated at the differential pair for large input signals. Moreover, transistors M_{3B}-M_{3C} and M_{4B}-M_{4C} in the RFC OTA are rearranged by applying the Local Common Mode Feedback (LCMFB) technique [23], which was previously explained in Chapter 2. This way, the drains of M_{3C} and M_{4C} are connected through two matched resistors with equal resistance $R_1 = R_2 = R$, thus feeding their common-mode voltage to the gates of transistors M_{3B} and M_{4B}. This technique allows further increase of the dynamic currents without scaling static currents. In absence of input signal, there is not voltage drop in R_1 and R_2, so M_{3A}-M_{3B} and M_{4A}-M_{4B} act as conventional current mirrors. However, for a large positive V_{id}, current I_{1B} in M_{1B} is lower than current I_{2B} in M_{2B}, leading to a voltage drop $\Delta V = R \cdot (I_{2B} - I_{1B})/2$ in R_1 and R_2. This voltage drop is added to the quiescent gate voltage of M_{3A} and subtracted from the quiescent gate voltage of M_{4A}, yielding a large output current leaving the OTA. Analogously, for a large negative V_{id} voltage drop $\Delta V = R \cdot (I_{2B} - I_{1B})/2$ is negative, leading to a large output current entering the OTA. Hence SR is improved without increasing quiescent currents.

Besides improved dynamic performance, LCMFB also increases small-signal performance thanks to the small-signal current gain provided by the LCMFB resistors and the AC small-signal ground at the common-gate of M_{3B}-M_{4B}. An in-depth analysis of the small-signal and large-signal operation of the super class AB RFC OTA is presented in following paragraphs.

Several choices can be made for the adaptive biasing of the differential pair in Figure 4.16(c). In Chapter 2.2.3.1, three possibilities were explained [1]. In this case, the two DC level shifters option has been chosen, due to its good performance, i.e. its well defined quiescent current, its increased dynamic current not limited by I_B and its doubled transconductance. However, a 50% extra bias current is used versus Figure 4.16(a) and Figure 4.16(b).

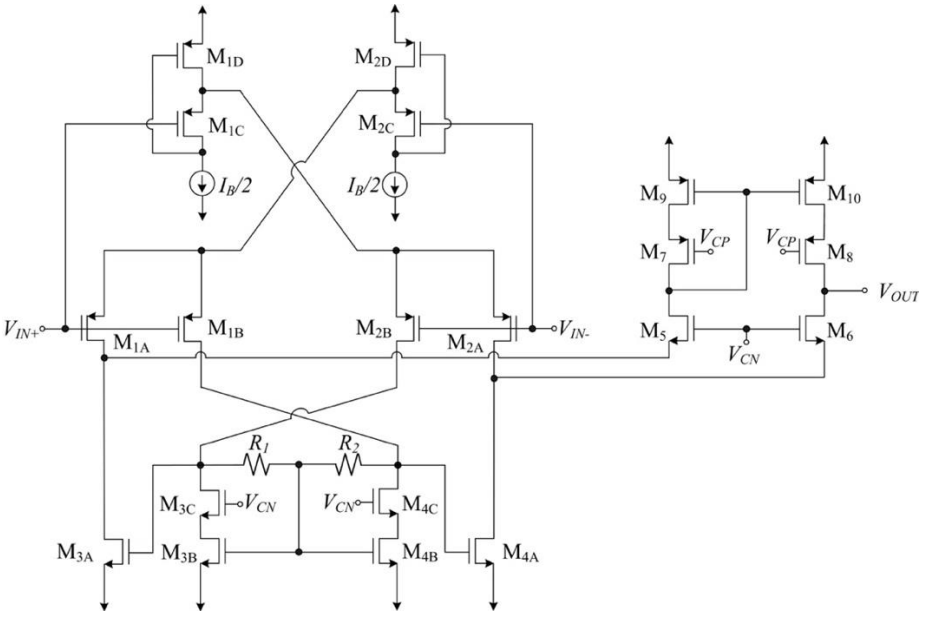

Figure 4.17. Detailed schematic of proposed super class AB RFC OTA

The minimum supply voltage of the OTA is $V_{DD,min} = |V_T|+3|V_{DS,sat}|$, with $|V_{DS,sat}|=|V_{GS}|-|V_T|$ the drain-source saturation voltage. Hence the circuit can operate at moderately low voltage. In fact, FVFs are suited to low supply voltage, since the drain voltage of $M_{1C,2C}$ is set to V_{DD}-$V_{SG1D,2D}$. Therefore, the input range of the FVFs in Figure 4.17 and thus the common-mode input range (CMIR) of the OTA is $|V_{TP}|-|V_{DS,sat1C}|$ to keep M_{1C}-M_{2C} in saturation. Note that it does not increase with the supply voltage. In the process employed V_{TP} = -0.96 V, so with $|V_{DS,sat1C}|$=0.1 V, CMIR = 0.86 V. The CMIR of the RFC OTA of Figure 4.16(a) is $V_{DD}-|V_{SS}|-2|V_{DS,sat}|-|V_{TP}|$, that for a 2 V supply leads to 0.84 V, a similar value. If a higher CMIR (and supply voltage) is required for the proposed OTA, a DC level shift made by a source follower can be included in the FVF loop [19].

If small-signal analysis is performed, the transconductance of conventional folded cascode OTA of Figure 4.16(a) is:

$$G_{mFC} = 2 \cdot g_{m1A} \tag{4.10}$$

and that of RFC is

$$G_{mRFC} = 2 \cdot g_{m1A}(1 + K) \tag{4.11}$$

Note that for the typical value K=3, G_{mRFC} is twice G_{mFC} using the same static power. The transconductance of the super class AB RFC OTA of Figure 4.17 is

$$G_{mAB} = 2 \cdot g_{m1A}[1 + g_{m3A}(R \| r_{o2B})] \tag{4.12}$$

with r_{o2B} the small-signal drain-source resistance of transistor M_{2B}. The factor 2 in Equation 4.12 is due to the extra transconductance provided by the adaptive bias circuit of the differential pair, and the factor $1+g_{m3A}(R||r_{o2B})$ is due to the LCMFB configuration. Note that choosing

$$R > \frac{K-1}{2g_{m3A}} \tag{4.13}$$

transconductance of the super class AB RFC OTA is larger than that of the RFC OTA, where it has been assumed that $R<<r_{o2B}$.

The output resistance of the FC OTA is

$$R_{oFC} \approx g_{m6}r_{o6}\left(\frac{r_{o2A} \| r_{o4A}}{2}\right) \| g_{m8}r_{o8}r_{o10} \tag{4.14}$$

and that of the RFC and super class AB RFC OTA is

$$R_{oRFC} = R_{oAB} \approx g_{m6}r_{o6}(r_{o2A} \| r_{04A}) \| g_{m8}r_{o8}r_{o10} \tag{4.15}$$

Hence, both the conventional RFC and super class AB RFC OTAs enhance low-frequency gain compared to the FC OTA due to the higher transconductance and output resistance. If design condition in Equation 4.13 is met, the super class AB RFC provides more gain than the RFC OTA due to the increased transconductance, which is also responsible for the same increase in GBW. Expressions for the GBW of the FC, RFC and super class AB RFC OTAs are:

$$GBW_{FC} = \frac{2g_{m1A}}{2\pi C_L} \tag{4.16}$$

$$GBW_{RFC} = \frac{(K+1)g_{m1A}}{2\pi C_L} \tag{4.17}$$

$$GBW_{AB} = \frac{2g_{m1A}}{2\pi C_L}[1 + g_{m3A}(R \| r_{o2B})] \tag{4.18}$$

Note that, as R increases, GBW of the super class AB RFC OTA also increases. However, larger values for the LCMFB resistors lead to a decrease in the non-dominant poles associated to the drain of M_{3C} and M_{4C}. Hence a tradeoff between GBW increase and phase margin degradation exists in the choice of R.

In addition, stability must be considered. The FC, RFC and super class AB RFC OTAs have a dominant pole ω_{p1} = -1/(R_{out} C_{out}) set by the output terminal, with $C_{out} \approx C_L$ the output capacitance of the OTA. They also have a non-dominant pole $\omega_{p2} \approx -g_{m5}/C_{p5}$ corresponding to the source terminals of M_5 and M_6, with C_{p5} the intrinsic capacitance at the source of M_5, which is C_{gs5} plus other smaller capacitances. In addition, the RFC introduces a pole- zero pair due to the active current mirrors M_{3A}-M_{3B} and M_{4A}- M_{4B}, $\omega_{p3} \approx -g_{m3B}/(C_{gs3A}+C_{gs3B})$ and $\omega_{z1} \approx -(1+K)\cdot\omega_{p3}$. Since this pole-zero pair is associated with NMOS devices, it is usually at relatively high frequency. However, large K values increase C_{gs3A} and thus decrease ω_{p3}. For this reason, practical K values in the RFC are around 2-4 [14].

In the proposed super class AB RFC, the virtual signal ground at the common gate of M_{3B}-M_{4B} cancels the effect of C_{gs3B} and C_{gs4B}, but R_1-R_2 increase the resistance at the nodes corresponding to the drain of M_{3C} and M_{4C}. Hence the non- dominant pole ω_{p3} becomes $\omega_{p3} \approx -1/[(R\|r_{o2B})C_{gs3A}]$ and is the lowest frequency non-dominant pole even for moderate R values, yielding a phase margin in this case:

$$PM \approx 90º - \tan^{-1}\left(\frac{GBW}{f_{p3}}\right) \approx$$

$$\approx 90º - \tan^{-1}\left\{2g_{m1A}(R\|r_{o2B})\frac{C_{GS3A}}{C_L}[1 + g_{m3A}(R\|r_{o2B})]\right\} \qquad (4.19)$$

Hence to get e.g. a target PM = 60º, the minimum load capacitance under these conditions is

$$C_{L,min} \approx 3.46 g_{m1A}(R\|r_{o2B})[1 + g_{m3A}(R\|r_{o2B})]C_{GS3A} \qquad (4.20)$$

Note from expression 4.19 that a large R value leads to a significant phase margin degradation. This has traditionally limited the performance of LCMFB schemes [23]. Fortunately, in super class AB OTAs it is not necessary to use large R values to achieve very high SR and current efficiency, since the adaptive biasing of the differential input pair allows large voltage drops at the resistors without requiring large resistance values or large static power consumption.

An analysis of the equivalent input noise of the FC, RFC, and super class-AB RFC OTAs is presented in Appendix B. Regarding thermal noise, note from this analysis that the higher DC gain of the RFC and super class AB RFC

reduces the influence of the transistors in the output branch on the input-referred noise, as expected. It is not possible to determine the topology with the lowest thermal noise, as it depends on g_m and R values chosen. However, just to have a numerical example, assuming that $g_{m1A} = g_{m3B} = g_{m9} = g_{m3A}/3$ and that $R = 10/g_{m3B}$, the RFC OTA and super class-AB RFC OTA have a 18% and 55% lower input-referred thermal noise than the FC OTA, respectively. A higher R value further decreases the input noise due to the increased DC gain, but it also degrades PM as described previously.

Concerning flicker noise, note from the analysis of Appendix B the reduction of flicker noise achieved in the super class-AB RFC OTA, which is due to the lower influence of the NMOS transistors (which generate the larger flicker noise) when the noise generated by them is referred to the input, thanks to the larger DC gain.

Besides small signal parameters, large-signal performance must be considered. A critical factor in the settling performance of the OTA is the SR. Assuming a capacitive load, it is given by SR=I_{omax}/C_{out}, with I_{omax} the maximum output current, and $C_{out} \approx C_L$ if as usually load capacitance C_L is much larger than the intrinsic capacitance at the output node. The SR of the FC OTA of Figure 4.16(a) is

$$SR_{FC+} = SR_{FC-} = \frac{2I_B}{C_L} \tag{4.21}$$

since the maximum current sourced to the load of sunk from it is $2I_B$. A symmetrical positive and negative slew is achieved, but the maximum output current is limited by the bias current. Hence a tradeoff between SR and static power consumption arises. The slew rate in the RFC OTA is approximately [14]

$$SR_{RFC+} = SR_{RFC-} = \frac{2KI_B}{C_L} \tag{4.22}$$

which is higher than for the FC OTA for K>1 but still experiencing the same tradeoff.

An approximate theoretical SR of the super class-AB RFC OTA of Figure 4.17 is deduced in Appendix C, yielding

$$SR_+ \approx \frac{\beta_{3A}}{2C_L}\left(\sqrt{\frac{\beta_{2B}}{2\beta_{3B}}}A + \frac{R_1\beta_{2B}}{4}A^2\right)^2 \tag{4.23}$$

$$SR_- \approx \frac{\beta_{4A}}{2C_L}\left(\sqrt{\frac{\beta_{1B}}{2\beta_{4B}}}A + \frac{R_2\beta_{1B}}{4}A^2\right)^2 \tag{4.24}$$

where A is the amplitude of the differential input step. Note that a large value not bound by I_B can be achieved.

Expressions 4.23 and 4.24 are a theoretical limit. In practice values of SR are lower since some transistors leave the saturation region for large input steps (e.g. by the limitation of drain voltage set by the cascode transistors) and due to second-order effects which are not accounted for in the simple MOS square law model. However, these expressions reflect that large SR can be achieved without increasing static power and show the main parameters influencing SR.

Amplifier design is application specific, so it is difficult to outline a generic design strategy. However, in most cases GBW, PM and SR are the key design criteria. Hence, Expressions 4.18, 4.19, 4.23 and 4.24 can be used as a starting point for a preliminary hand-calculation design of a super class AB RFC OTA. Common design practices can be used for choosing the transistor aspect ratios [14]. Thus, input transistors M_{1A}-M_{1C} and M_{2A}-M_{2C} have typically large aspect ratio and are biased in moderate or even weak inversion to increase GBW and minimize input offset and noise. Moreover, this choice also reduces their $|V_{DS,sat}|$, maximizing CMIR as previously discussed. A critical design choice is the value of R, as it represents a tradeoff between increase of GBW, SR, reduction of input noise and increase of PM and silicon area. For a given power budget (hence I_B), C_L and minimum PM (defined in Expression 4.19) can be used to estimate the maximum R, which can then be used in Equation 4.18 to estimate the GBW and (to a first order approach) the SR using Expressions 4.23 and 4.24. This procedure can be the starting point to refine the R value and aspect ratios during computer simulations.

The super class AB RFC of Figure 4.17 was fabricated in the same 0.5 μm double-poly, 3-metal n-well CMOS technology that was previously employed for the other OTAs. Both the FC and RFC OTAs of Figure 4.16(a) and Figure 4.16(b) were also fabricated on the same test chip prototype for

comparison purposes. The three OTAs were available on the chip in both open loop and in unity-gain closed-loop configuration. Resistors R_1 and R_2 were made by a high resistance polysilicon layer available in the technology. They have a nominal value of 10 kΩ and were interdigitized and surrounded by dummy strips for improved matching. Similar conventional matching techniques were also used for the transistors. A microphotograph of the three OTAs is shown in Figure 4.18, where their relative area requirements can be observed. The transistor dimensions employed are summarized in Table 4.4.

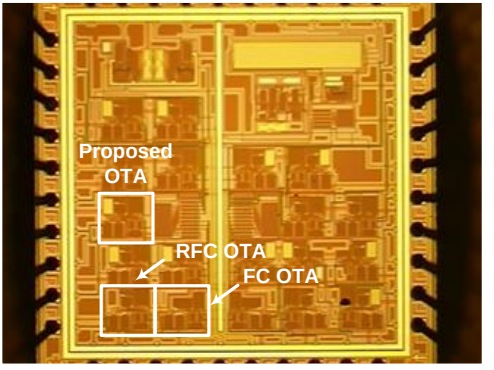

Figure 4.18. Test chip microphotograph of the OTAs of Figure 4.16

Transistor	**W/L** (μm/μm)
M_{1A}-M_{2A}	190/0.6
M_{1B}-M_{2B}	190/0.6
M_{1C}-M_{2C}	190/0.6
M_{1D}-M_{2D}	60/0.6
M_{3A}-M_{4A}	180/0.6
M_{3B}-M_{4B}	60/0.6
M_{3C}-M_{4C}	60/0.6
M_5-M_6	120/0.6
M_7-M_8	200/0.6
M_9-M_{10}	200/0.6

Table 4.4. Transistor aspect ratio of OTAs in Figure 4.16 and Figure 4.17

The supply voltages employed in all the measurements were ±1 V, and the bias current I_B was 10 µA. Externally applied cascode bias voltages V_{CP} and V_{CN} were set to -0.5 V and 0.3 V, respectively. An off-chip ceramic load capacitor of 47 pF was connected to the output of the OTAs for measurements. As the OTA outputs were directly connected to bonding pads and the test probe is connected without a buffer, the total load capacitance is increased by the pad, board and test probe capacitance. The estimated total value of C_L is hence of approximately 70 pF.

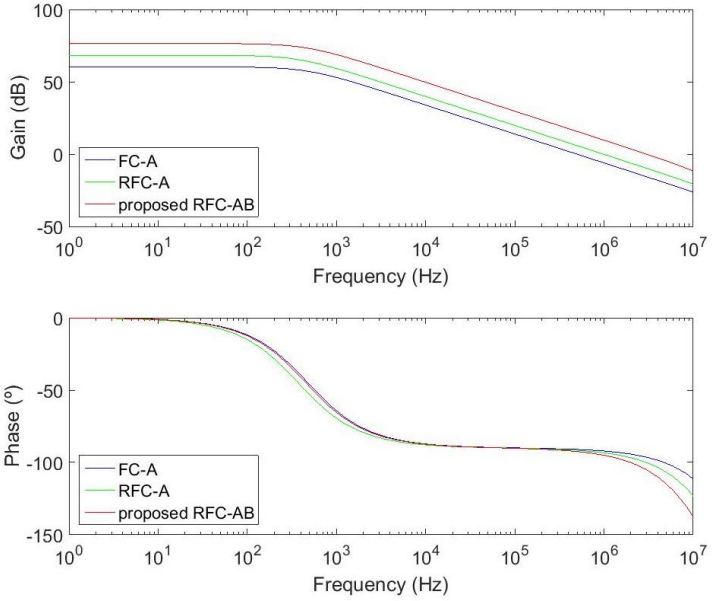

Figure 4.19. Simulated AC open loop response of the FC, RFC and super class AB RFC OTAs

Figure 4.19 shows the simulated open loop AC small signal response of the amplifiers. The DC gains of the FC, RFC and super class AB RFC are 60.3 dB, 68.4 dB and 76.8 dB, respectively. Note the increased value of the super class AB RFC OTA versus the RFC OTA due to the LCMFB technique, as expected. The GBW of the FC, RFC and super class AB RFC is 500.7 kHz, 975 kHz and 3 MHz, respectively. Hence the super class AB RFC OTA shows an increase in GBW by a factor 6 when compared to the FC OTA and about 3 versus the RFC OTA. The phase margin (PM) of FC, RFC and super class AB RFC is 89º, 86.7º and 75.1º, respectively. At 3 MHz the PM of the RFC OTA is

79.6º so the super class AB RFC OTA leads to a degradation of 4.5º for the reason previously described.

Figure 4.20 shows the measured output current of the three OTAs for a differential input voltage ranging from -0.2 V to 0.2 V. Measurements have been done using the configuration shown in Figure A.3(a) of Appendix A. Note that the output current of the FC and RFC OTA is limited by the bias current as they operate in class A. The super class AB RFC OTA features much larger output currents for large input signals, not limited by the bias current.

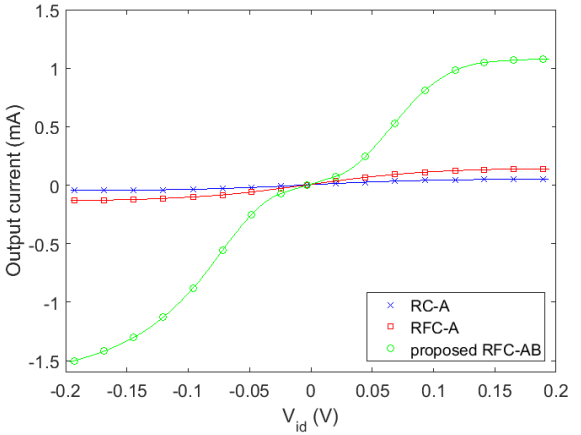

Figure 4.20. Measured output current of the FC, RFC and super class AB RFC OTAs vs differential input voltage

The measured response the OTAs using a 1 MHz 0.5 V periodic square wave with DC level of -0.3 V at the input is shown in Figure 4.21, as well as the input waveform. Note the faster settling of the proposed super class AB RFC OTA, without noticeable ringing. The measured SR+ for the FC OTA and RFC OTA is 0.20 V/µs and 0.38 V/µs, respectively. The measured SR_+ for the super class AB RFC OTA is 13.2 V/µs, which corresponds to an increase factor of 66 and 34.7 versus the FC and RFC OTAs, respectively, for the same quiescent current and C_L. An 8% undershoot is observed at the falling edge, which is attributed to the adaptive biasing when it operates with very low input voltages. Note however that the output is damped in a cycle, denoting the stable closed-loop operation of the amplifier. No overshoot/undershoot is observed for small input steps, as expected from the PM of 75.1º.

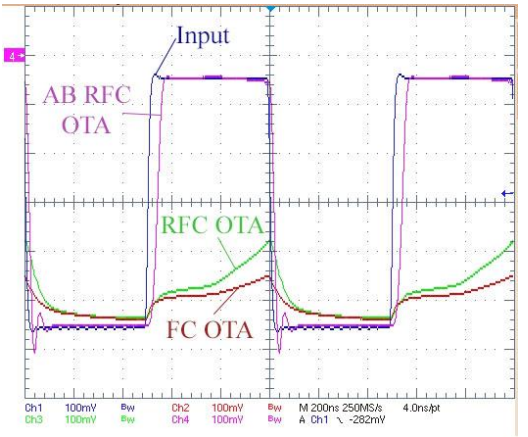

Figure 4.21. Measured response of the FC, RFC and super Class AB OTAs to a square input signal

Figure 4.22 shows the measured Total Harmonic Distortion (THD) of the three OTAs for an input sinusoid of 25 kHz and peak-to-peak amplitude ranging from 200 mV to 1 V. Note that the proposed super class AB RFC OTA achieves the lowest distortion, which is attributed to the higher DC open-loop gain and the improved settling performance. The main contribution to distortion in the three OTAs is due to the second harmonic, as expected for a single-ended output topology.

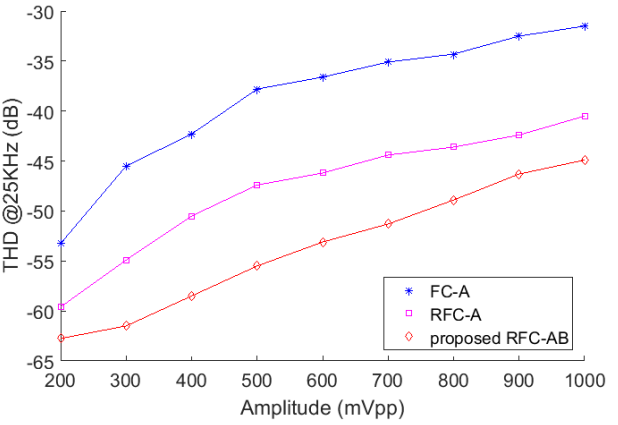

Figure 4.22. Measured THD vs input amplitude of the FC, RFC and super class AB RFC OTAs

A summary of the main measurement results obtained for the three OTAs is provided in Table 4.8, also including data for other OTAs reported to date for comparison. GBW is approximated by the measured bandwidth of the OTAs in unity-gain configuration, since the non-dominant poles are beyond the unity-gain bandwidth. Note that the proposed OTA improves both small signal and large-signal performance, in agreement with the analysis presented before. Increase in the measured GBW versus the value in simulation for the proposed OTA is mainly attributed to process variations of the poly resistors implementing *R*. Parameters like CMRR, PSRR and equivalent input noise density are enhanced mainly due to the higher DC gain of the proposed OTA. The drawbacks are the lower value of the phase margin, the 25% extra quiescent power consumption due to the added current sources $I_B/2$ in the adaptive biasing, and a 15% extra silicon area due to the adaptive biasing and the resistors. It is also possible to scale down by a factor *n* transistors M_{1C} and M_{2C}, scaling by the same factor the FVF bias current and leading to just a $25/n$ % extra power.

Thus, a simple modification of the recycling folded cascode OTA has been proposed, which leads to a super class AB implementation. The use of adaptive biasing of the differential pair and LCMFB leads to improved small-signal and large- signal performance. Measurement results show a significant increase in SR and GBW fast settling. The OTA can be employed in low voltage low power circuits requiring a good performance/power tradeoff.

Some simple variations of the basic super class AB RFC OTA of Figure 4.17 can be made, which can be useful in certain applications. They are briefly addressed in the following paragraphs.

The first modification is shown in Figure 4.23. Here the adaptive biasing of the input pair is removed. The main advantage is the reduced static power consumption versus the OTA of Figure 4.17. However, the small-signal and large-signal performance are worse. In this case, dynamic current boosting only relies on the use of LCMFB.

The transconductance of OTA in Figure 4.23 is half that of OTA in Figure 4.17 (defined by Equation 4.12), as factor 2 was caused by the adaptive biasing circuit of the differential pair that is not present now. Thus, GBW of the amplifier in Figure 4.23 is half that of Figure 4.17. The output resistance of the OTA is the same as that of OTA in Figure 4.17 (see Equation 4.15).

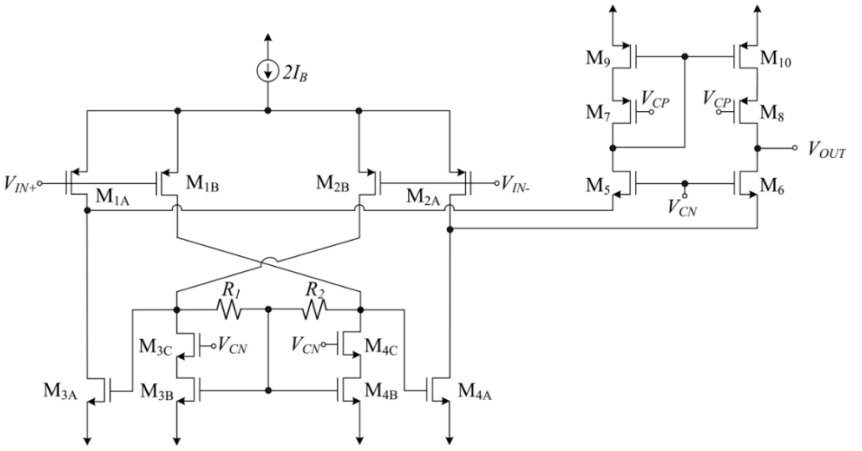

Figure 4.23. RFC without adaptive biasing scheme at the input pair

As it happened with OTA in Figure 4.17, the value of the gain bandwidth product (GBW) can be increased by making *R* larger. However, the phase margin gets worse, limiting the value of *R*. Hence, there is a tradeoff between GBW and stability. The main shortcoming is that without adaptive biasing of the differential pair, it is difficult to get large voltage drops at the resistors without using large *R* values, so the achievable SR for a given phase margin is significantly lower than in Figure 4.17.

Two different versions of circuit in Figure 4.23 were fabricated in a 0.5 μm CMOS technology, with R = 10 kΩ and R = 20 kΩ, respectively. They were fabricated in both open loop and buffer configuration. The aspect ratios of transistors for both OTAs are shown in Table 4.5. As in previous measurements, the bias current is set to 10 μA, and cascode voltages V_{CP} and V_{CN} are -0.5 V and 0.3 V, respectively. External 47 pF capacitors are used as load, which added to the pad, board and test probe capacitances leads to an estimated total value of C_L of approximately 70 pF.

Figure 4.24 depicts the transient response for both circuits when a 0.5 V_{pp} 100 kHz sinusoidal signal is applied to the input, with an input common mode voltage of -0.3 V. Note that the OTA with R = 20 kΩ shows improved SR, but also a small ringing in the falling edge, denoting the decreased phase margin due to the higher R value. Although their THD values are not very high, OTA with R = 20 kΩ presents better THD than OTA with R = 10 kΩ (-42.5 dB vs -39.8 dB for a 50 kHz 0.4 V_{pp} sinusoidal input). Open loop parameters are included in Table 4.8

Transistor	**W/L** (μm/μm)
M_{1A}-M_{2A}	190/0.6
M_{1B}-M_{2B}	190/0.6
M_{1C}-M_{2C}	190/0.6
M_{1D}-M_{2D}	60/0.6
M_{3A}-M_{4A}	180/0.6
M_{3B}-M_{4B}	60/0.6
M_{3C}-M_{4C}	20/0.6
M_5-M_6	40/0.6
M_7-M_8	50/0.6
M_9-M_{10}	40/0.6

Table 4.5. Aspect ratio of transistors of Figure 4.23

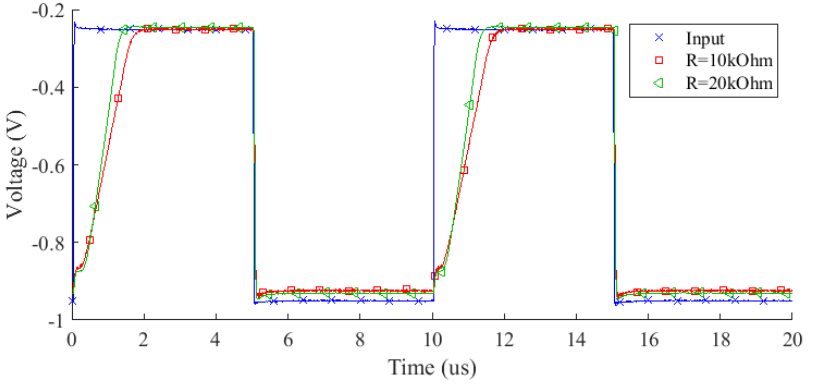

Figure 4.24. Transient response of OTA in Figure 4.23 with R=10 kΩ and R=20 kΩ

A second variant of circuit in Figure 4.17 is obtained by replacing transistor M_8 with a QFG-MOS transistor (previously explained in Section 2.1.2). Figure 4.25 depicts the schematic of the modified circuit. The circuit acts as that of Figure 4.17 in quiescent conditions, while in dynamic conditions, the adaptive biasing of the cascode transistors M_7-M_8 allows avoiding a constant V_{DS} in M_9-M_{10} that would make M_9-M_{10} enter triode region for large output currents. The main shortcoming is that die area is increased due to capacitor C_{BAT}.

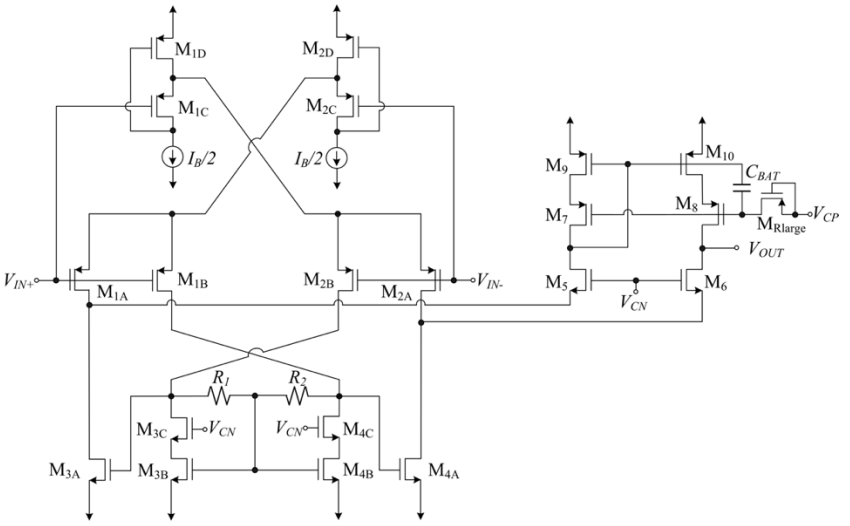

Figure 4.25. RFC with QFG MOS transistor

In order to compare them, circuits in Figure 4.17 and Figure 4.25 were fabricated with the same transistor dimensions included in Table 4.5. Capacitor C_{BAT} was fabricated on chip, with a value of 1 pF and transistor M_{Rlarge} has an aspect ratio of 1.5 µm/600 nm. The measured transient response of both OTAs to a 0.5 V_{pp} 100 kHz sinusoidal input signal, with V_{CMin} = -0.3V, is shown in Figure 4.26. The resulting SR values of OTAs in Figure 4.17 and Figure 4.25 are 6 V/µs and 9.7 V/µs, respectively, obtaining an improvement factor of 1.6.

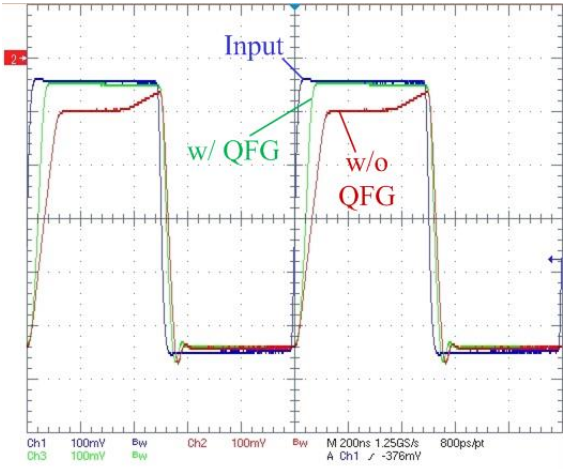

Figure 4.26. Transient response of OTAs of Figure 4.17 and Figure 4.25

As for the open loop parameters, both circuits present the same values, which are included in Table 4.8, since the QFG transistor has no impact in DC.

As it has been observed in this Section, the performance of the super class AB RFC OTA of Figure 4.17 strongly relies on the resistance value R of two matched passive resistors, which can suffer from process and temperature variations. Moreover, R can be chosen to optimize SR, GBW and phase margin for a given load capacitance C_L. Since R is fixed once the OTA is fabricated, the use of a different C_L leads to a suboptimal performance. Moreover, R in Figure 4.17 was implemented using a high resistance non-silicided polysilicon layer which may not be available in some low-cost CMOS processes.

A simple modification which solves these issues is proposed in Figure 4.27. Active resistors replace these passive resistors, leading to a more flexible approach able to adapt to process and temperature variations and to different load conditions, and requiring less silicon area and no high resistive layer.

In this design, local common mode feedback is implemented by matched transistors M_{R1}-M_{R2} operating in triode region as active resistors. When the differential input signal is null, there is no current flowing through M_{R1}-M_{R2} and the circuit in Figure 4.27 behaves as the RFC OTA in Figure 4.16(b), with the same well-defined quiescent currents. However, with a differential input voltage $V_{id} > 0$, there are identical voltage drops in M_{R1} and M_{R2} leading to an increase in the V_{GS} of M_{3A} and a decrease in the V_{GS} of M_{4A}, thus causing a large output current flowing to the load. For negative differential input voltages ($V_{id} < 0$), a large current sinks from the load due to the decrease in $V_{GS,3A}$ and the increase of $V_{GS,4A}$.

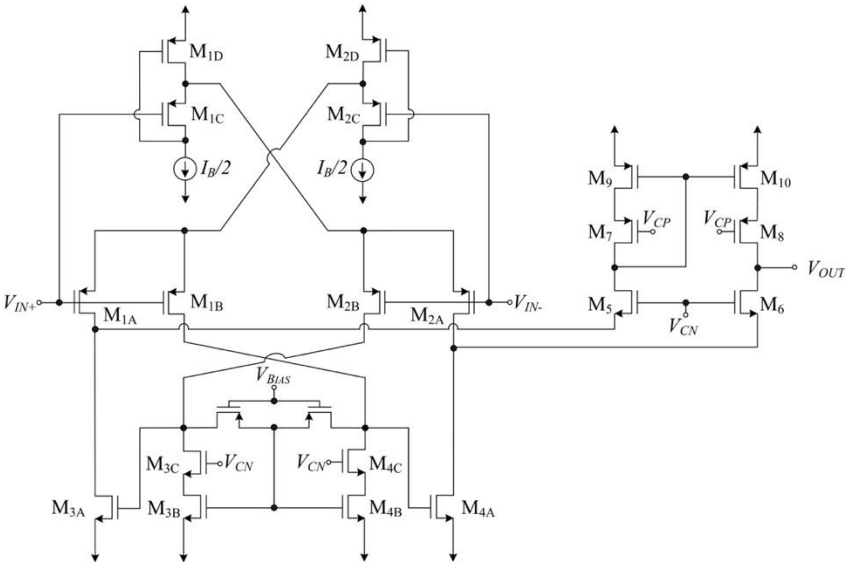

Figure 4.27. Class AB RFC with variable LCMFB resistors

The expressions for the GBW and SR of the OTA in Figure 4.27 are:

$$GBW \approx \frac{2g_{m1A}}{2\pi C_L}[1 + g_{m3A}R_{DS}] \tag{4.25}$$

$$SR \approx \frac{\beta_{3A,4A}}{2C_L}\left(\sqrt{\frac{\beta_{1B,2B}}{2\beta_{3B,4B}}}A + \frac{R_{DS}\beta_{1B,2B}}{4}A^2\right)^2 \tag{4.26}$$

being A the amplitude of the differential input step and R_{DS} the drain source resistance of M_{R1} and M_{R2}, which is controlled by DC voltage V_{BIAS}:

$$R_{DS} \approx \frac{1}{\beta_{R1,2}(V_{BIAS}-V_{G,3B}-V_{TH})} = \frac{1}{\beta_{R1,2}\left(V_{BIAS}-\sqrt{\frac{I_B}{\beta_{3B}}}-V_{SS}-2V_{TH}\right)} \tag{4.27}$$

Note that the larger R_{DS}, the greater GBW and SR, but at the same time, PM is degraded, as it happened in the OTA of Figure 4.17. For moderately large R_{DS} (few kΩ) the lowest non-dominant pole (gate node of $M_{3A,4A}$) becomes $\omega_{pND} \approx -1/(R_{DS} \cdot C_{gs3A})$ and the phase margin is defined by:

$$PM \approx 90º - \tan^{-1}\left(\frac{GBW}{f_{pND}}\right)$$

$$\approx 90º - \tan^{-1}\left\{2g_{m1A}R_{DS}\frac{C_{gs3A}}{C_L}[1 + g_{m3A}R_{DS}]\right\} \tag{4.28}$$

Thus, adjusting V_{BIAS} (hence R_{DS}) not only permit the optimization of GBW, SR and PM for a given C_L but also the compensation from process or temperature variations.

A test chip prototype was fabricated in the previous 0.5 µm CMOS process including the OTAs of Figure 4.16(a), Figure 4.16(b) and Figure 4.27. Transistor aspect ratios are those previously used and listed in Table 4.4. The aspect ratio of M_{R1} and M_{R2} is 30 µm/1 µm. Figure 4.28 shows the microphotograph of the OTA of Figure 4.27. Supply voltage was ±1 V, I_B = 10 µA, V_{CP} =-0.5V and V_{CN} = 0.3V. An external load capacitor of 47 pF was employed, which added to the capacitance of the test setup (pad, board and test probe) leads to $C_L \approx 70$ pF.

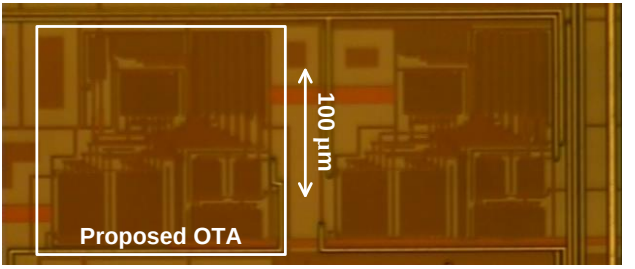

Figure 4.28. Microphotograph of the OTA of Figure 4.27

The simulated GBW and PM for V_{BIAS} between 0.6 V and 0.9 V is plot in Figure 4.29. As expected from Expressions 4.25, 4.26 and 4.28, GBW is inversely proportional to V_{BIAS} and PM decreases for lower V_{BIAS} (i.e., larger R_{DS}).

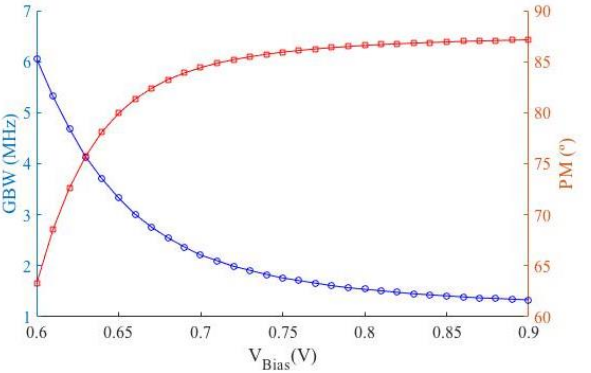

Figure 4.29. GBW and PM vs V_{BIAS}

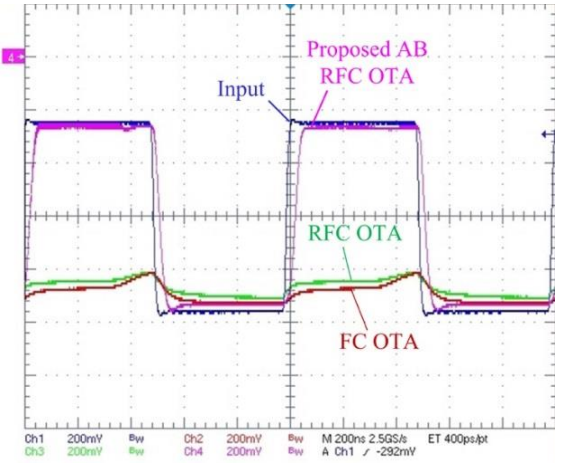

Figure 4.30. Transient response

The transient response of the three OTAs in unity-gain configuration was measured. It is shown in Figure 4.30. The input signal is a 1 MHz 0.5 V_{pp} periodic square wave with -0.6 V DC level and V_{BIAS} = 660 mV. The SR of the OTA of Figure 4.27 is highly improved if it is compared with the conventional FC OTA and the RFC proposed in [14]. The performance of the three OTAs are summarized in Table 4.8. Note the improved small and large signal performance at the expense of slightly lower PM and 20% extra quiescent power of the adaptive biasing circuit.

Another possible variation of OTA in Figure 4.17 is using non-linear current mirrors instead of LCMFB at the folding stage. This is reflected in the following figure. The extra dynamic current boosting at the active load of the differential pair is achieved by changing the bias voltage of the cascode transistors M_{3C}-M_{4C}. This new bias voltage V_{BIAS} is chosen so that in quiescent conditions (i.e. with current I_B flowing through M_{3B}- M_{3C} and M_{4B}-M_{4C}) transistors M_{3B} and M_{4B} operate in saturation, but close to the ohmic region (with V_{DS} slightly larger than $V_{DS,sat}$=V_{GS}-V_{TH}). Hence, in quiescent and small-signal conditions M_{3A}-M_{3B} and M_{4A}-M_{4B} act as linear current mirrors. However, when V_{id} > 0, current I_{2B} in M_{2B} increases, which increases $V_{GS,3C}$. This way, $V_{DS,3B}$ decreases, driving M_{3B} into triode region. As a result, the gate voltage of M_{3A}-M_{3B} increases notably, yielding a large current in transistor M_{3A} (which is in saturation region) that is conveyed to the output by M_5 and M_7-M_{10}.

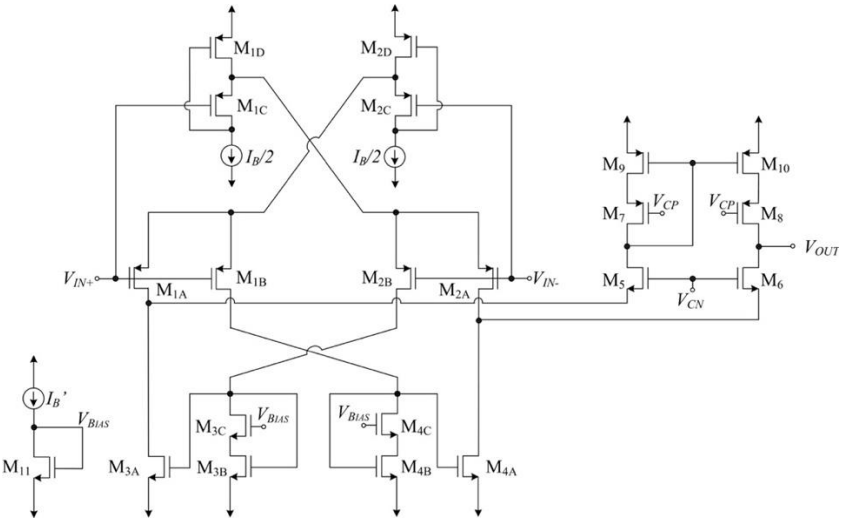

Figure 4.31. Class AB RFC with non-linear current mirror at the load stage

An approximate analytical expression for the output current I_{out} when $V_{id} > 0$ can be obtained using the simple square-law MOS model for strong inversion and saturation region and the expression for ohmic region and low V_{DS} given by $I_D = \beta \cdot (V_{GS} - V_{TH}) \cdot V_{DS}$. The resulting current in M_{3A} is

$$I_{3A} = \frac{\beta_{3A}}{2}\left(\frac{I_{2B}}{\beta_{3B} V_{DS,3B}}\right)^2 \tag{4.29}$$

where $V_{DS,3B} = V_{BIAS} - \sqrt{2I_{2B}/\beta_{3C}} - V_{TH}$. Expressing I_{2B} as a function of V_{id}, current I_{3A} becomes

$$I_{3A} = \frac{\beta_{3A}}{2}\left[\frac{\beta_{2B}}{2\beta_{3B} V_{DS,3B}}\left(\sqrt{\frac{I_B}{\beta_{1B}}} + V_{id}\right)^2\right]^2 \tag{4.30}$$

For a large positive differential input step of A Volts current in M_{1A} and M_{4A} is very low and M_{2A} enters deep triode region, so $I_{out} \approx I_{3A}$ and

$$SR_+ \approx \frac{\beta_{3A}}{2C_L}\left[\frac{\beta_{2B}}{2\beta_{3B} V_{DS,3B}} A^2\right]^2 \approx \frac{K}{8C_L}\frac{\beta_{2B}^2}{\beta_{3B} V_{DS,3B}^2} A^4 \tag{4.31}$$

Analogously, for $V_{id} < 0$:

$$I_{4A} = \frac{\beta_{4A}}{2}\left[\frac{\beta_{1B}}{2\beta_{4B} V_{DS,4B}}\left(\sqrt{\frac{I_B}{\beta_{2B}}} + V_{id}\right)^2\right]^2 \tag{4.32}$$

and for a large negative differential input step of -*A* Volts, $I_{out} \approx I_{4A}$ and

$$SR_{-} \approx \frac{\beta_{4A}}{2C_L}\left[\frac{\beta_{1B}}{2\beta_{4B}V_{DS,4B}}A^2\right]^2 \approx \frac{K}{8C_L}\frac{\beta_{1B}^2}{\beta_{4B}V_{DS,4B}^2}A^4 \tag{4.33}$$

In practice SR is lower due to second-order effects not considered in the analysis and since transistors operating in saturation may leave this region for large inputs. Note however that a large SR compatible with low static power is achieved as SR is not proportional to I_B.

A simple and robust way to generate V_{BIAS} is shown in Figure 4.31. Choosing I_B' and the *W/L* of M_{11} correctly, $V_{DS3B,4B}$ can be set slightly above $V_{DS,sat}$ regardless of process, temperature or supply voltage variations as V_{BIAS} is set by the V_{GS} of a scaled replica of M_{3B}-M_{4B}.

The adaptive bias current source employed also improves GBW, as the full differential input signal is applied to each input transistor [1].

OTAs of Figure 4.16(a), Figure 4.16(b) and Figure 4.31 were included on a 0.5 μm CMOS chip prototype. The aspect ratio of every transistors except for M_{11} are that on Table 4.4, and that of M_{11} is 15 μm/0.6 μm. Figure 4.32 shows a microphotograph of the three OTAs. Supply voltage was set to ±1V, $I_B = I_B' = 10$ μA, $V_{CP} = -0.5$ V and $V_{CN} = 0.3$ V.

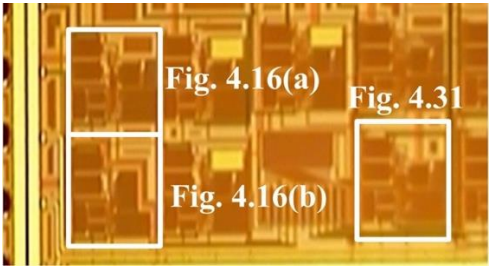

Figure 4.32. Microphotograph of OTAS in Figure 4.16(a), Figure 4.16(b) and Figure 4.31

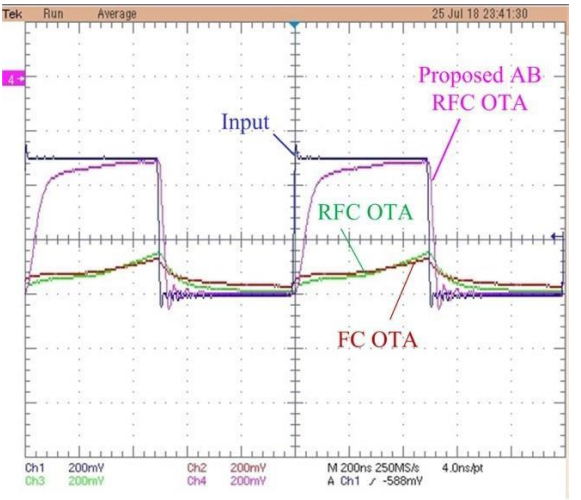

Figure 4.33. Transient response of OTAs of Figure 4.16(a), Figure 4.16(b) and Figure 4.31

The measured transient response in voltage follower configuration of the three OTAs is shown in Figure 4.33. An external load capacitor of 47 pF was connected. However, including the capacitance of the test setup (pad, board and test probe), the overall load capacitance is $C_L \approx 70$ pF. The input signal was a 1 MHz 0.5 V periodic square wave, whose DC level was -0.6 V. Table 4.8 summarizes the main measured performance parameters. Note an improved SR by a factor of 28 versus the FC OTA.

In addition, the figures of merit previously defined are included in Table 4.8. Note that the proposed OTA shows competitive small-signal and large-signal performance.

Thus, proper biasing of the differential pair active load in the RFC OTA can provide dynamic current boosting in a simple way. Together with an adaptive biasing current source, efficient super class AB operation can be achieved.

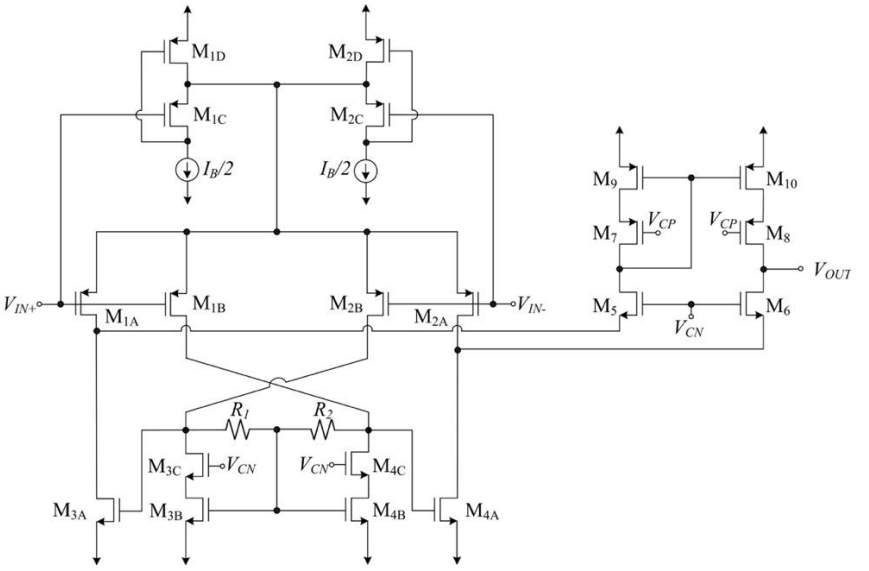

Figure 4.34. Class AB RFC with WTA scheme at the input stage

Another alternative topology is obtained by modifying the adaptive biasing scheme of Figure 4.17 by a Winner-Take-All (WTA) configuration, previously explained in Chapter 2. Figure 4.34 shows the complete schematic of this amplifier. As it was mentioned in Section 2.2.3.2, dynamic currents achieve with the WTA scheme are the same as that of cross-coupled floating batteries, hence the same SR equation of Figure 4.17 applies in this case (see expression 4.23 and 4.24). However, since the common source node behaves as a virtual ground, the transconductance is not improved when compared with conventional class A amplifier. Thus, the transconductance (so as GBW) of op-amp of Figure 4.34 is half of that of Figure 4.17, i.e. GBW = $g_{m1A}\cdot[1+g_{m3A}(R\|r_{o2B})]$, which leads to a 6 dB decrease in the DC gain.

Transistors sizes of this OTAs are that in Table 4.4. Supply voltages are set to ± 1V, and bias current I_B is 10 μA. Cascode voltages V_{CP} and V_{CN} are -0.5 V and 0.3 V respectively.

The transient response of the Class A Folded Cascode, conventional Class A RFC and the amplifier of Figure 4.34 to a 0.5 V_{pp} 1 MHz square signal was measured and plot in figure below. The input common mode is V_{CMin} = -0.6 V. It can be seen that the transient response of the amplifier of Figure 4.34 is improved, but settling performance is worse than with the previously used adaptive biasing scheme. This may be due to the lower speed of

the WTA circuit for large inputs (which can drive M_{1D} and M_{2D} near triode region).

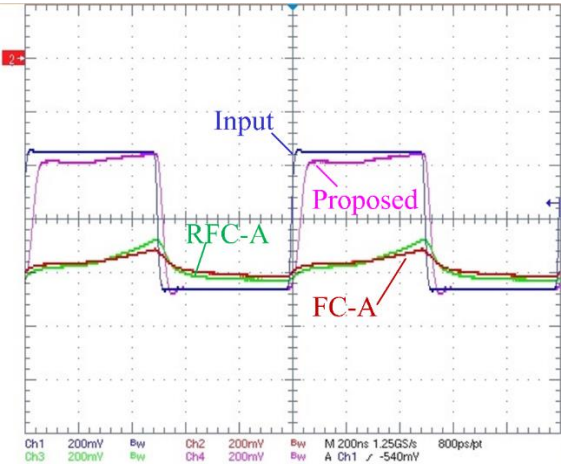

Figure 4.35. Transient response of the WTA class AB RFC

As for the small signal parameters, the simulated values are included in Table 4.8. As it was mentioned before, the A_{DC} is 6 dB below that of Figure 4.17 and GBW is half of that of Figure 4.17.

Another variation of the amplifier of Figure 4.17 is depicted in Figure 4.36. In this case, the drains of transistors M_{1A} and M_{2A} are not connected to that of M_{3A} and M_{4A}, but to that of M_{1B} and M_{2B}, respectively. Since they are connected in parallel, they behave as a single transistor with twice the size. In addition, the dimensions of M_{3A}, M_{3B}, M_{4A} and M_{4B} have been changed so that the power consumption of OTA of Figure 4.36 is the same as that of Figure 4.16(a), that is, now the four transistors have the same dimensions. The resulting circuit corresponds to the conventional super class AB (symmetrical current mirror) OTA [1].

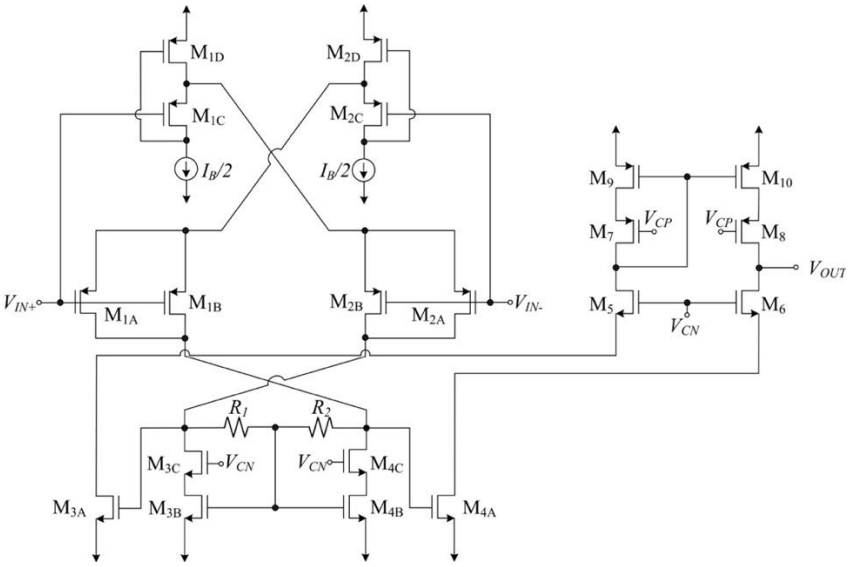

Figure 4.36. An alternative super class AB RFC OTA

The transconductance, output resistance and *GBW* of the above amplifier are

$$G_m = 2(g_{m1A} + g_{m1B})g_{m3A}(R\|r_{o2A}\|r_{o2B}) = 4g_{m1A}g_{m3A}(R\|(r_{o2B}/2)) \quad (4.34)$$

$$R_{out} \approx g_{m6}r_{o6}r_{o4A}\|g_{m8}r_{o8}r_{o10} \quad (4.35)$$

$$GBW = \frac{4g_{m1A}g_{m3A}(R\|(r_{o2B}/2))}{2\pi C_L} \quad (4.36)$$

Although there is an increase factor of 2 when comparing Equations 4.34 and 4.12, g_{m3A} is $\sqrt{2}/3$ of the g_{m3A} of Figure 4.17, so the net factor is $2\sqrt{2}/3=0.94$ due to the resizing. Note that $R\|(r_{o2B}/2)$ can be as low as half of the value of $(R\|r_{o2B})$, depending of the value of R and r_{o2B}. Since the value of R cannot be increased with no limit, due to the non-dominant pole introduced by the active current mirror ($\omega_{p3} \approx -1/[(R\|r_{o2B})C_{gs3A}]$) usually $R<<r_{o2B}$ and similar values of G_m (thus *GBW*) can be obtained for both amplifiers in Figure 4.17 and Figure 4.36.

As for the output resistance, that of Figure 4.36 is greater than that of Figure 4.17, since the term r_{o2B} disappeared and r_{o4A} is larger since M_{4A} drives 2/3 less quiescent current in Figure 4.36. Thus, higher values of A_{DC} can be achieved.

With a transient analysis similar to that of Appendix C, it can be deduced that the theoretical value of the SR is

$$SR \approx \frac{\beta_{3A}}{2C_L}\left(\sqrt{\frac{\beta_{2B}}{\beta_{3B}}}A + \frac{R_1\beta_{2B}}{2}A^2\right)^2 \tag{4.37}$$

In order to compare this expression with Equations 4.23 and 4.24, the value of β_{3A} in Figure 4.17 and Figure 4.36 are related as follows: $\beta_{3A,17} = 3\cdot\beta_{3A,36}$. Hence, the following expression is obtained for the OTA of Figure 4.17:

$$SR \approx \frac{\beta_{3A,36}}{3C_L}\left(\sqrt{\frac{\beta_{2B}}{2\beta_{3B,36}}}A + \frac{R_1\beta_{2B}}{2}A^2\right)^2 \tag{4.38}$$

It can be deduced that with high values of amplitude, larger *SR* can be obtained for the same power consumption.

The OTA of Figure 4.36 was fabricated in the same 0.5 µm CMOS technology which has been used previously, along with the FC and conventional RFC amplifiers. Table 4.6 contains the dimensions of the transistors.

Transistor	**W/L** (µm/µm)
M_{1A}-M_{2A}	190/0.6
M_{1B}-M_{2B}	190/0.6
M_{1C}-M_{2C}	190/0.6
M_{1D}-M_{2D}	60/0.6
M_{3A}-M_{4A}	120/0.6
M_{3B}-M_{4B}	60/0.6
M_{3C}-M_{4C}	120/0.6
M_5-M_6	120/0.6
M_7-M_8	200/0.6
M_9-M_{10}	200/0.6

Table 4.6. Transistors aspect ratio of opamp in Figure 4.36

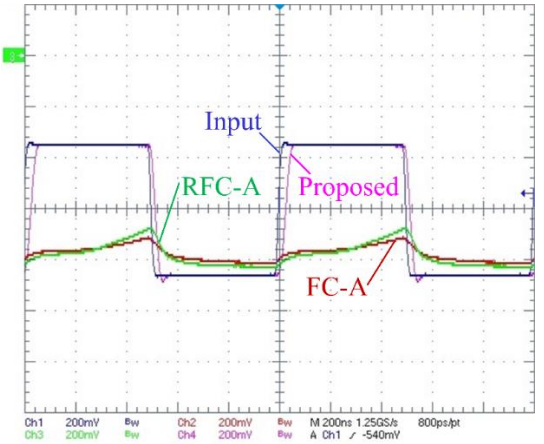

Figure 4.37. Transient response of the amplifier in Figure 4.36

The transient response of the amplifier in Figure 4.36 is plot in Figure 4.37, along with that of conventional FC and RFC OTAs. The input voltage was a 1 MHz 0.5 V_{pp} square signal, with an input DC level of V_{CMin} = -0.6 V. As it can be seen in figure above, the proposed circuit can follow the input signal, whereas the conventional FC and RFC class A amplifiers cannot. Note that the amplitude of the output signal reaches the maximum amplitude, i.e. that of the input signal.

Finally, Figure 4.38 shows the last alternative to the RFC of Figure 4.17. Despite the improved small-signal and large-signal performance of the super class AB RFC OTA in Figure 4.17, it is still limited by various reasons. First, cascode transistors are biased with constant voltages, which limits the V_{DS} of the transistors connected to their source and that therefore can make these transistors enter triode region for large dynamic currents. This fact can restrict the maximum dynamic currents and hence degrade SR notably [27]. The modification in Figure 4.25 alleviates this problem but cascode transistors M_5 and M_6 are still biased with constant voltage. Second, the bottom current mirrors still scale the quiescent currents by factor *K*. The amplifier proposed in Figure 4.38 overcomes these drawbacks, improving both small-signal and large-signal performance for the same quiescent power consumption and supply voltage requirements.

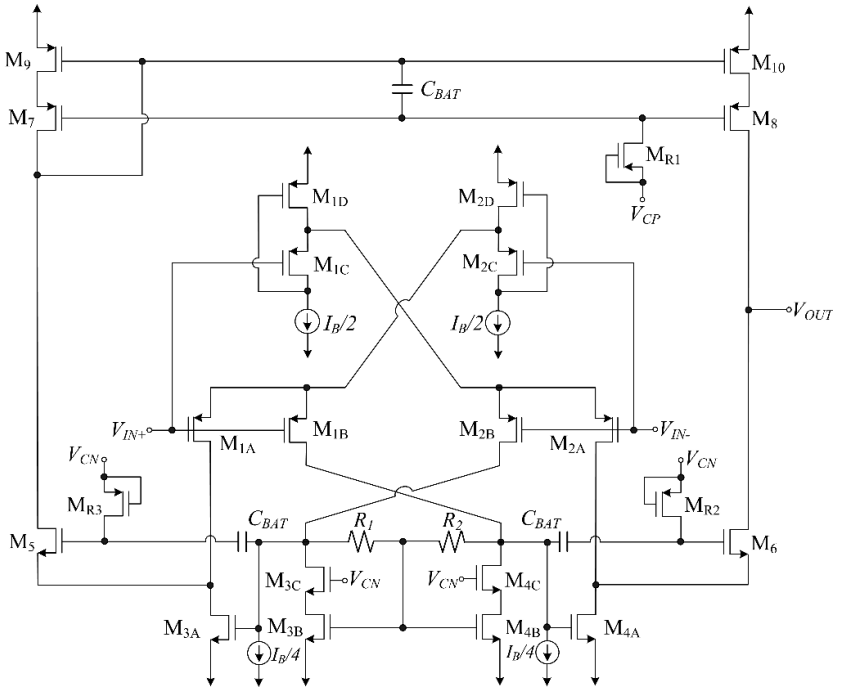

Figure 4.38. Enhanced super class AB RFC OTA

Two main improvements are included versus the OTA in Figure 4.17. First, based on [15], current mirrors $I_B/4$ are connected to the drains of M_{1B} and M_{2B}. This reduces the quiescent current of M_{3B}-M_{4B} from $I_B/2$ to $I_B/4$, allowing to use a K=6 (instead of K=3) at the bottom current mirrors M_{3A}-M_{3B} and M_{4A}-M_{4B} for the same quiescent current consumption. As a result, the expressions for transconductance and GBW of the OTA in Figure 4.38 are the same as that of the OTA in Figure 4.17. (see Expressions 4.12 and 4.18). However, an increase factor of 1.41 is obtained, since g_{m3A} increases by the same factor. Hence this modification improves small-signal performance preserving quiescent currents.

The second improvement concerns large signal operation. The theoretical positive and negative SR of the RFC in Figure 4.17 are defined by Expression 4.23 and 4.24, respectively. However, in practice lower values are achieved mainly because transistors M_{3A}, M_{4A}, M_9 and M_{10} may enter triode region for large A values. This is due to cascode transistors M_5, M_6, M_7 and M_8 which restrict their V_{DS}. This limitation is very relevant with the low supply voltages employed nowadays in advanced technology nodes, which notably

restrict the maximum cascode bias voltages. The solution employed here is the use of dynamic biasing of the cascode transistors using Quasi-Floating Gate (QFG) techniques [20], [27], as shown in Figure 4.38. Three capacitors C_{BAT} are included that connect the gates of M_{3A}-M_5, M_{4A}-M_6 and $M_{9,10}$-$M_{7,8}$. Minimum-size PMOS transistors M_{P1}, M_{P2} and M_{P3} act as high resistance pseudo-resistors for DC biasing of the cascode transistors. In quiescent operation capacitors C_{BAT} behave as open circuits and no current flows through the pseudo-resistors, so cascode bias voltages are V_{CP} and V_{CN}, just like in Figure 4.16(b). However, for a large positive differential input voltage, the voltage at the gate of M_{3A} increases. Since C_{BAT} cannot discharge fast, it acts as a floating battery that translates this voltage increase to the gate of M_5. This way the V_{DS} of M_{3A} increases, allowing to drive a large current without entering triode region. Similarly, the decrease of the gate voltage of M_9-M_{10} produced by this large current is translated to the gate of M_7-M_8, increasing the V_{SD} of M_9-M_{10}. For a large negative differential input voltage, the voltage at the gate of M_{4A} increases and this increase is translated to the gate of M_6, leading to a larger V_{DS} in M_{4A} that allows sinking a large current from the load as M_{4A} does not enter triode region.

Both amplifiers of Figure 4.16(b) and Figure 4.38 were designed and fabricated in a GlobalFoundries 130 nm 8-metal CMOS technology. Resistors R_1 and R_2 of 20 kΩ were made by a high resistance silicided polysilicon layer available in the technology. Conventional matching enforcement techniques were used for the transistors and resistors. Dual nitride MiM capacitors with nominal capacitance of 500 fF were used to implement C_{BAT}. A chip microphotograph is shown in Figure 4.39. Since the top passivation layer is opaque in this process, the designed layout has been superimposed. Transistor aspect ratios are summarized in Table 4.7.

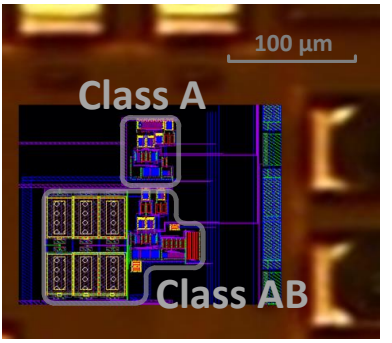

Figure 4.39. Test chip microphotograph

The OTAs of Figure 4.16(b) and Figure 4.38 were measured in unity-gain closed loop configuration using a dual supply voltage of ±0.5 V and a bias current I_B = 3 µA.

Transistor	**W/L** (µm/µm)
M_{1A}-M_{2A}	12/0.24
M_{1B}-M_{2B}	12/0.24
M_{1C}-M_{2C}	12/0.24
M_{1D}-M_{2D}	12/0.24
M_{3A}-M_{4A}	72/0.24
M_{3B}-M_{4B}	12/0.24
M_{3C}-M_{4C}	12/0.24
M_5-M_6	24/0.24
M_7-M_8	12/0.12
M_9-M_{10}	12/0.24
M_{R1}, M_{R2}, M_{R3}	0.16/0.12

Table 4.7. Transistor Aspect Ratios of opamps of Figure 4.16(b) and Figure 4.38

For time-domain measurements, an external ceramic load capacitor of 47 pF was connected to the output. The total capacitance also includes the capacitance of the pad, package traces, PCB plating bus and active probe, and its estimated value is C_L = 70 pF. For frequency-domain measurements, the same 47 pF ceramic capacitor was used at the output, but now an external wideband buffer was employed. Hence the total capacitance includes the load, pad,

package traces, PCB plating bus and buffer input capacitances. The total estimated value is C_L = 50 pF.

Figure 4.40 shows the response of the RFC OTA of Figure 4.16(b) and the super class AB RFC OTA of Figure 4.38 to a 1 MHz 0.4 V periodic square input signal, also shown in the figure. The DC input level was set to 0 V. Note the improved dynamic performance of the proposed OTA of Figure 4.38. The measured average SR = (SR_++SR_-)/2 of the RFC OTA of Figure 4.16(b) is 0.194 V/μs and that of the proposed OTA of Figure 4.38 is 19.26 V/μs, i.e., almost 100 times higher.

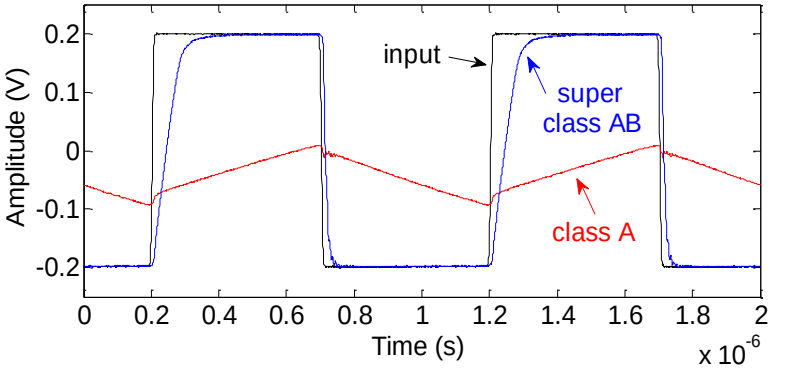

Figure 4.40. Measured response of the RFC and super class RFC OTAs to a square input signal

The frequency response of both circuits as voltage followers is shown in Figure 4.41. The measured bandwidth corresponds to the OTA unity-gain frequency and to the GBW since the non-dominant poles are above this frequency. The circuit of Figure 4.16(b) has a f_{-3dB}= 380 kHz and the circuit of Figure 4.38 has a f_{-3dB}= 10.43 MHz, i.e., an increase factor of 27.

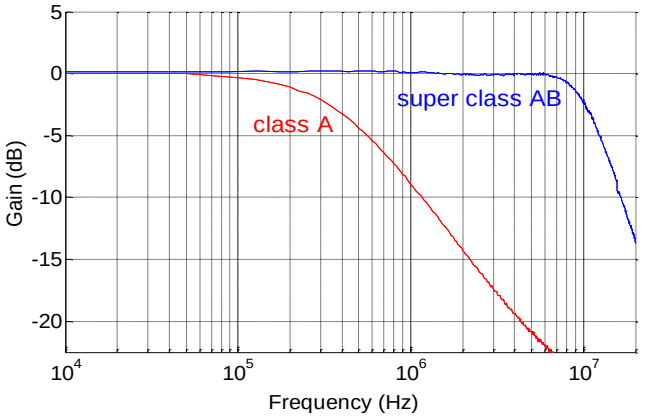

Figure 4.41. Measured frequency response of both OTAs connected as voltage followers

The measured Total Harmonic Distortion (THD) of both circuits is shown in Figure 4.42. A single input tone of 10 kHz and peak-to-peak amplitude ranging from 100 mV to 450 mV has been used. The low frequency employed is due to the low bandwidth of the class A RFC OTA of Figure 4.16(b) which does not allow comparison at high frequencies. Note that the OTA of Figure 4.38 achieves lower distortion, mainly due to the increased transconductance achieved, as previously mentioned.

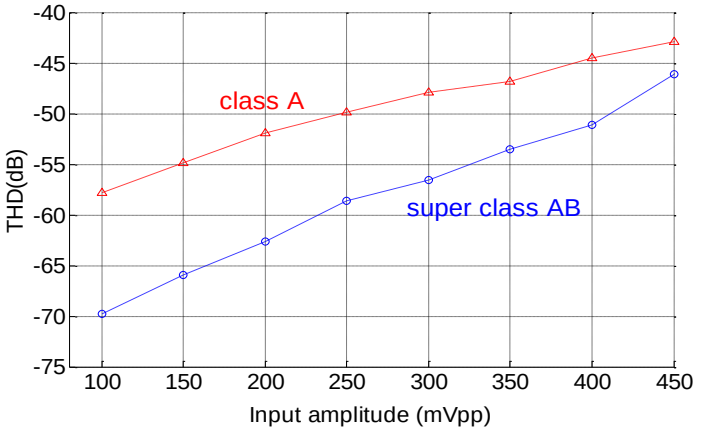

Figure 4.42. Measured THD vs input amplitude of the RFC and super class AB RFC OTAs

The main measurement results of both OTAs are included in Table 4.8. Note the improved small-signal and large-signal operation of the proposed super class AB RFC OTA. To allow a simpler comparison, the previously defined Figures of Merit have been employed. Note that the proposed OTA shows improved performance for both FoMs. The drawbacks of the proposed circuit are the increased area requirements (mainly due to capacitors C_{BAT}) and a 25% increase in static power consumption versus the RFC OTA of Figure 4.16(b).

4.2 Comparison of the Class AB Amplifiers

In this Chapter, several amplifiers have been proposed, all of them with different features. The purpose of this section is to compare them and highlight their benefits and disadvantages, and their possible applications. Besides, other amplifiers previously published have been included in order to put together the state of the art and have a global point of view.

Table 4.8 sums up the parameters of the different op-amps. Note that four different technologies have been employed to fabricate the amplifiers: 0.5 μm, 0.35 μm, 0.18 μm and 0.13 μm. Besides, amplifiers proposed in [7], [8] and [26] employ differential topologies, which present higher G_m when compared to their respective single-ended version.

As for the SR, the greater value is obtained by [26]. However, its power consumption is much higher (in the order of mW) than the ones in this thesis (around 100 μW). Among the amplifiers proposed in this work, the amplifier of Figure 4.27 presents the higher SR, due to its adaptive local common-mode feedback (LCMFB) scheme, making this alternative a flexible solution. For fixed R_{LCMFB} schemes, Figure 4.17, Figure 4.34 and Figure 4.36 achieve also very large output currents.

Regarding the small signal parameters, the amplifier in [26] has the greatest GBW, but again, its power consumption is much higher. If the amplifiers proposed in this thesis are considered, the opamp of Figure 4.38 has the greatest GBW, due to the fact that it was fabricated in a 0.13 μm. For a 0.5 μm technology, the circuit proposed in Figure 4.8 has the biggest GBW and A_{DC} values of the proposed topologies. However, its transient behavior is not as good as other proposed OTAs, such as Figure 4.17. This fact makes amplifier in

Figure 4.8. Proposed class AB folded cascode OTA

suitable for applications which requires a good small-signal performance, while not needing large dynamic output currents.

For a more understandable comparison, the two figures of merit previously employed are calculated for every amplifier: a large-signal FoM, $FoM_L = SR \cdot C_L/I_{supply} = I_{maxL}/I_{supply}$, where I_{supply} is the total current consumption, which represents the large-signal current efficiency, and a small-signal FoM, $FoM_S = 100 \cdot GBW \cdot C_L/I_{supply}$ (MHz·pF/μA), which shows the small-signal speed/power ratio. Figure 4.43 represents both large and small signal Figures of Merit for the amplifiers in Table 4.8. Logarithmic axes are employed so that the points are clearly shown. For both FoMs, the higher values, the better performance the amplifier has. Thus, the target is to place the amplifiers in the upper right corner. As it can be seen from that figure, the FoM values of the proposed amplifiers are higher than those of the state of the art. Note the great improvement achieved by the amplifier of Figure 4.38, due to the use of a 0.13 μm technology. This fact confirms that the advantages of the proposed techniques (mainly tested in a 0.5 μm process) also apply in more modern technology nodes.

The small-signal FoM of Figure 4.23 and Figure 4.34 are lower than the rest of the proposed amplifiers. The reason of their relatively low FoM_S is that they do not use adaptive biasing techniques which double the transconductance. In the case of Figure 4.23 (with and without QFG), they use a conventional transistor acting as current source, and Figure 4.34 uses a WTA scheme, which provides large dynamic current but it does not increase the G_m.

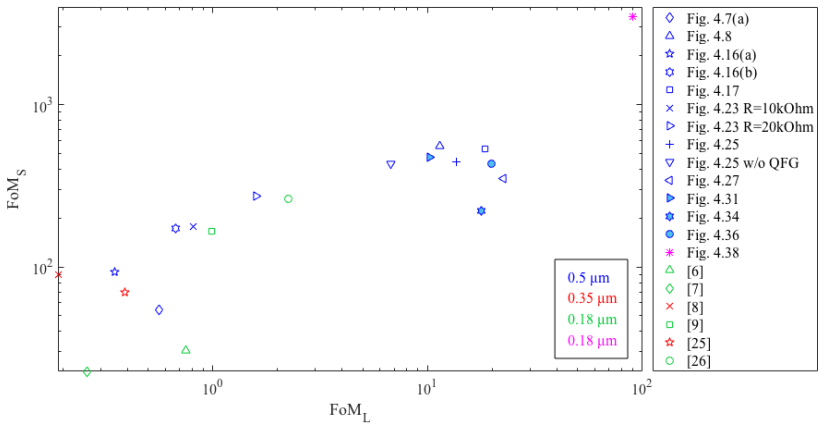

Figure 4.43. Performance comparison using two FoM

	CMOS tech. (µm)	C_L (pF)	*SR+* (V/µs)	*SR-* (V/µs)	t_{settl+} *(ns)*	t_{settl-} *(ns)*	*THD (dB)*	A_{DC}* *(dB)*	*PM** (°)	*GBW (MHz)*	*Eq. input noise** *@1MHz* (nV/√Hz)	*Power* (µW)	*Area* (mm²)	FoM_L	FoM_S
Figure 4.7(a)	0.5	70	0.32	-0.28	--	--	-24 @100kHz 1 V_{pp}	69	89	0.31	49	80	0.020	0,56	54.3
Figure 4.8	0.5	70	9.8	-7.6	96	74	-41 @100kHz 1 V_{pp}	81.7	60	4.75	35	120	0.024	11.43	554
Figure 4.16(a)	0.5	70	0.20	-0.66	2700	1840	-37.8 @ 25 kHz 0.5 V_{pp}	60.3	89	0.53	22	80	0.022	0.35	92.8
Figure 4.16(b)	0.5	70	0.38	-1.5	1720	560	-47.4 @ 25 kHz 0.5 V_{pp}	68.4	86.7	0.98	19	80	0.026	0.67	171.5
Figure 4.17	0.5	70	13.2	-25.3	120	100	-55.5 @ 25 kHz 0.5 V_{pp}	76.8	75.1	3.8	15	100	0.030	18.48	532
Figure 4.23 R=10k	0.5	70	0.46	-20.1	1400	107	-47.3 @ 25 kHz 0.5 V_{pp}	68.7	86.3	1.01	36	80	0.028	0.81	176.8
Figure 4.23 R=20k	0.5	70	0.91	-24.3	920	165	-50.2 @ 25 kHz 0.5 V_{pp}	73.4	80.1	1.57	35	80	0.028	1.59	274.8
Figure 4.25 w/ QFG	0.5	70	10.2	-16.5	380	94.4	-57.02 @ 25 kHz 0.5 V_{pp}	77.6	77.4	3.19	22.8	100	0.026	13.58	446.6
Figure 4.25 w/o QFG	0.5	70	6.9	-14.5	496	101	-56.94 @ 25 kHz 0.5 V_{pp}	77.6	77.6	3.10	22.8	100	0.025	6.72	434
Figure 4.27	0.5	70	16.04	-18.2	--	--	-45.5 @ 25 kHz 0.5 V_{pp}	76.4	81.3	2.5	23	100	0.025	22.46	350

	CMOS tech. (µm)	C_L (pF)	SR+ (V/µs)	SR- (V/µs)	t_{settl+} (ns)	t_{settl-} (ns)	THD (dB)	A_{DC}* (dB)	PM* (º)	GBW (MHz)	Eq. input noise* @1MHz (nV/√Hz)	Power (µW)	Area (mm^2)	FoM_L	FoM_S
Figure 4.31	0.5	70	7.27	-18.8			-47.85 @ 25 kHz 0.5 V_{pp}	75.1	76.3	3.4	22	100	0.02	10.18	476
Figure 4.34	0.5	70	12.7	-23.1	420	130	-48.54 @ 25 kHz 0.5 V_{pp}	70.7	84.5	1.57	31.4	100	0.028	17.78	220
Figure 4.36	0.5	70	14.2	-26.8	90	71	-56.1 @ 25 kHz 0.5 V_{pp}	78.8	72.4	3.1	21	100	0.028	19.88	434
Figure 4.38	0.13	70/ 50	3.72	-34.8			-51 @ 10 kHz 0.4 V_{pp}	56.7	88.8	10.43	41	15	0.002	89.88	3477
[6]	0.18	8	0.14	--	--	--	-52 @ 1 kHz, 0.5 V_{pp}	51	60	0.057	--	1.2	0.057	0.75	30.4
[7]	0.18	20	2.89	--	--	--	-40 @ 0.4 V_{pp}	52	--	2.5	80	110	0.026	0.26	22.7
[8]	0.35	15	2.53	-1.37	224	--	--	88.3	66.1	11.67	<60	197	0.157	0.19	88.9
[9]	0.18	20	1.8	-3.8	1300	1000	-40.1 @250 kHz 0.4 V_{pp}	57.5	60	3	100	25.4	0.020	0.99	165.4
[25]	0.5	25	2.7	-3.3	--	--	-47.1 @ 2 V_{pp}	63.4	83	4.9	--	437.5	0.029	0.39	70
[26]	0.18	200	74.1	--	--	--	--	72	50	86.5	--	11900	0.070	2.24	261.7

*Simulation

Table 4.8. Summary of measurement results and performance

4.3 Conclusions

In this chapter, different single-ended amplifiers have been proposed. They are based on three of the most important OTA topologies: the telescopic cascode amplifier, the folded cascode and the recycling folded cascode. Different mathematical analysis were developed to prove the enhancement in different parameters, such as DC gain, GBW, SR and noise.

Different prototype chips were fabricated in two technologies (0.5 μm and 0.13 μm) in order to provide experimental measurements. All of them improve the performance of the conventional amplifiers.

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Chapter 5

FULLY DIFFERENTIAL CLASS AB AMPLIFIERS

In Chapter 4, several single-ended amplifiers have been presented. However, fully differential topologies present some advantages versus their single-ended version. Some of these benefits are:

- Increased gain

Thanks to the change in phase between the differential outputs, the amplitude of the output swing is doubled (i.e. an increase of 6 dB in voltage gain) over a single-ended output, thus improving also dynamic range. This is a clear positive point for low-voltage systems.

- Improved common-mode rejection ratio (CMRR)

Ideally, the effect of the common-mode input voltage appears equally at both output terminals, so it is cancelled out in the differential output voltage.

- Increased immunity to external noise and improved power supply rejection ratio (PSRR)

When signals are routed from one place to another, noise is coupled into the wiring. In differential systems, keeping the transport wires as close as possible to one another makes the noise coupled into the conductors appear as a common-mode voltage. Besides, noise that is common to the power supplies also appears as a common-mode output voltage, assuming perfect matching.

Since the differential amplifier rejects common-mode voltages, the system is more immune to external noise.

- Reduction in even-order harmonics

Expanding the transfer function of circuits into power series is a typical approach to quantify the distortion products. Taking a generic expansion of the outputs and assuming matched amplifiers:

$$V_{out+} = k_1 V_{in} + k_2 V_{in}^2 + k_3 V_{in}^3 + \cdots \quad (5.1)$$

$$V_{out-} = k_1(-V_{in}) + k_2(-V_{in})^2 + k_3(-V_{in})^3 + \cdots \quad (5.2)$$

Taking the differential output, the resulting expression is:

$$V_{od} = 2k_1 V_{in} + 2k_3 V_{in}^3 + \cdots \quad (5.3)$$

where k_i are constants. Thus, ideally, even terms disappear. In real life, they are reduced but not totally cancelled.

On the other hand, fully differential amplifiers (also known as FDA) have drawbacks: they are more complex as they need a common-mode feedback (CMFB) circuit in order to control the common-mode output voltage, leading to an increase in power consumption and in die area [1].

In this chapter, some power-efficient fully differential amplifiers are proposed. Section 5.1 presents a Common Mode Feedback circuit that has been improved by applying the Local Common-Mode Feedback technique. Then, a single-stage super class AB amplifier is shown in Section 5.3, making use of the proposed LCMFB circuit. After that, a micropower amplifier based on adaptive biasing and class AB current followers is proposed in Section 5.4 . Section 5.5 contains the last enhanced amplifier, which is the differential version of one of the RFC topologies proposed in Chapter 4. As it happened in the previous chapter, there is a final section to compare all the amplifiers treated in this chapter, besides other amplifiers previously published. To sum up, some conclusions are drawn in Section 5.7.

5.1 Improved common-mode feedback circuit

The block diagram of a fully differential amplifier (FDA) with CMFB is shown in Figure 5.1. The common-mode voltage V_{CM} is obtained by the common-mode sensor (CMS) and compared with a reference voltage (V_{CMREF}). The existing error $V_{CME} = V_{CM} - V_{CMREF}$ is amplified by the error amplifier (EA) and frequently transformed into a common-mode current I_{CM} that corrects the common-mode output voltage V_{CM}.

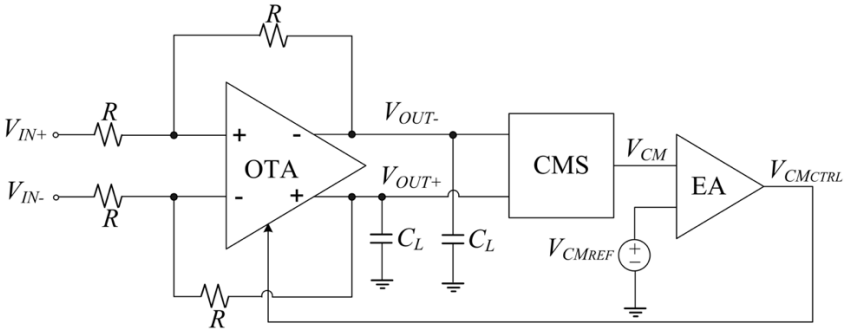


Figure 5.1. Block diagram of a fully differential amplifier with CMFB

Almost every CMFB circuit can be assorted into three groups:

a) Switched capacitor (SC) CMFB: they use matched capacitors to average the output voltage adjust the CM output. The main drawback they present is that they suffer from clock feedthrough, so they are not suitable for continuous time applications.

b) Resistor-averaged CMFB: two matched resistors are employed to average the output voltages. The resulting voltage is applied to a differential amplifier. Linearity and output range are improved but the resistors load the output, decreasing gain.

c) Differential difference amplifier (DDA) CMFB: a DDA (with two differential pairs at the input stage) [2] is used to simultaneously sense V_{CM}, compare it with V_{CMREF} and amplify the difference, without resistively loading the output. A conventional DDA CMFB is shown in Figure 5.2(a).

There are two relevant parameters that must be considered when designing a CMFB circuit: the gain-bandwidth product (GBW) and the transconductance gain, defined by $G_{M\_CMFB} = \delta I_{CM}/V_{CME}$. According with [3], these parameters should be maximized, as a large G_{M_CMFB} reduces the

common-mode offset voltage V_{CME}, providing a faster response, and a large GBW improves rejection of common-mode noise and interference at high frequencies.

In order to increase $G_{M\_CMFB,}$ a single-stage EA with high gain or a two-stage EA are normally used. Nevertheless, requirements on supply voltage or power consumption are higher, in addition to stability problems. To solve this issue, there are several alternatives to compensate the CMFB loop, but each one has its own drawbacks: an increase in the load capacitance C_L (decreasing the differential mode BW), a decrease on the CMFB loop gain (degrading accuracy) and the addition of an extra *RC* compensation network into the CMFB loop (complicating the design in both differential and common mode) [4].

The conventional DDA CMFB circuit is the most used one in continuous-time differential circuits. Its schematic is presented in Figure 5.2(a). When the common-mode output voltage V_{CM} is the same as the reference voltage V_{CMREF}, equal current I_B goes through transistors M_5 and M_6. Assuming that aspect ratio of M_7 and M_8 is the same as M_5, current I_{CM}, that controls the common-mode output voltage in the FDA, is set to I_B. If for instance there is a decrease in V_{CM}, current through M_6 also suffers a small decrease that depends on V_{CME}, satisfying $I_{d6}=I_{d1}+I_{d4}=I_B - \delta I$, while M_5 increases the same amount ($I_{d5}=I_{d2}+I_{d3}= I_B + \delta I$). This latter current is copied to M_7 and M_8, yielding an increase in V_{CM}. The implementation of M_5 and M_6 as diode connected transistors makes the non-dominant pole move to higher frequencies, thus improving stability. Besides, currents I_{CM} are generated more accurately, because they are defined by a current mirror.

Despite being the most used CMFB circuit, this topology has limitations in terms of G_{M_CMFB} ($G_{M\_CMFB} = 2g_{m1\text{-}4}$) and maximum output current ($\delta I_{MAX} = I_B$), limiting settling time of V_{CM}.

An alternative CMFB circuit is shown in Figure 5.2(b). The active load of the FDA has been replaced by a PMOS mirror, increasing its transconductance to $G_{M\_CMFB} = 2R_{out\_CM}.g_{m1\text{-}4}.g_{m7,8}$, with $R_{out\_CM} = r_{o2}\|r_{o3}\|r_{o5}$, thus there is an increase factor of $2R_{out\_CM}.g_{m7,8}$ comparing to the conventional CMFB circuit.

The problem with this topology is that the non-dominant pole decreases its frequency due to the increase of the resistance at the drains of M_5 and M_6, causing a strong reduction in the phase margin.

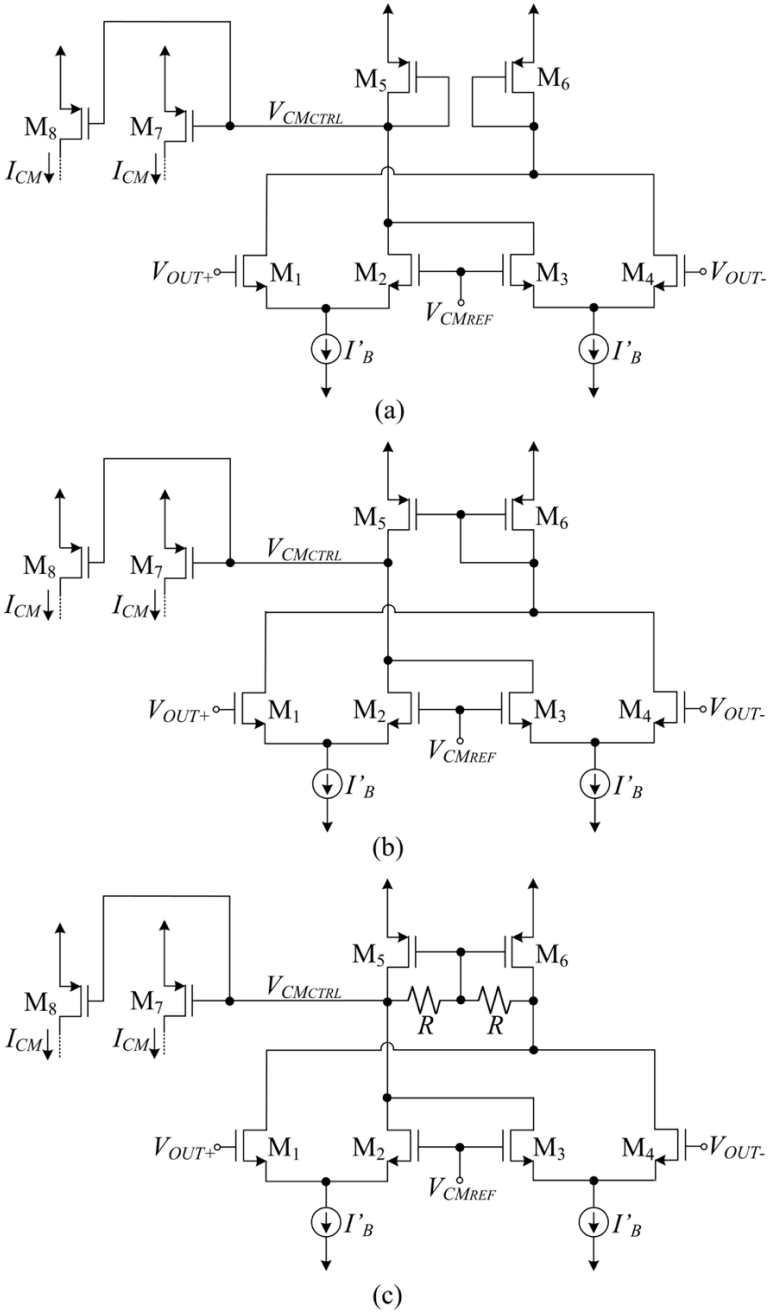


Figure 5.2. DDA-based CMFB (a) Conventional (b) Alternative (c) Proposed

Figure 5.2(c) presents the proposed CMFB that solves these drawbacks. A local common-mode feedback scheme is used as active load, instead of diode-connected active loads or a current mirror load [5]. Two matched resistors R are connected between the drain of M_5 and M_6, obtaining their common-mode voltage at the intermediate node. This voltage is then fed back to the common gate of M_5 and M_6. If $V_{CM} = V_{CMref}$, identical currents go through M_5 and M_6 ($I_5 = I_6 = I_B$), thus no current flows through resistors R. Hence, well controlled quiescent currents $I_{CM} = I_B$ are copied by current mirroring as in conventional CMFB. Nevertheless, if V_{CM} decreases and unbalances the DDA currents ($I_{d2}+I_{d3}= I_B + \delta I$ and $I_{d1}+I_{d4}=I_B-\delta I$), currents in M_5 and M_6 are still I_B (assuming that $R << r_{o5,6}$) and current δI goes through the resistors R. Thus, V_{CMctrl} is increased by $R\cdot\delta I$, leading to a dynamic current larger than I_B in M_7 and M_8, which is approximately:

$$I_{d7,8} = \frac{\beta_{7,8}}{2}\left(\sqrt{\frac{2I_B}{\beta_{5,6}}} + R\cdot\delta I\right)^2 \tag{5.4}$$

being $\beta_i = \mu C_{ox}(W/L)_i$ the transconductance factor of transistor M_i. As this current is larger, the charge or the load capacitors is faster, improving the settling of V_{CM} back to V_{CMREF}. Likewise, if V_{CM} increases, currents I_{d7} and I_{d8} decrease more quickly because of the voltage drop at the resistor, making the load capacitors discharge faster, thus improving dynamic performance.

When a small-signal variation v_{cm} is present in the common-mode output voltage, it causes a small-signal current through the resistors $i_R=2g_{m1}v_{cm}$, thus $G_{M\_CMFB} = 2Rg_{m1\text{-}4}g_{m7,8}$. If this parameter is compared with conventional CMFB circuit in Figure 5.2(a), an increase factor of $R\cdot g_{m7,8}$ is obtained, also applied in the GBW. Note that this factor is smaller than one of Figure 5.2(b), because $R << r_{o5,6}$, but at the same time, the decrease in the phase margin is smaller too, as the resistance at the drains of M_5 and M_6 is smaller.

If M_7 and M_8 are connected to the output branch of a FDA as additional current sources in order to inject I_{CM}, the open loop DC gain of Figure 5.2(c) follows the expression $A_{DC} = 2Rg_{m1\text{-}4}g_{m7,8}R_{out}$ where R_{out} is the output resistance of the FDA. The load capacitance C_L introduces the dominant pole at $f_d = 1/(2\pi R_{out}C_L)$. In addition, a non-dominant pole is at the output of the DDA circuit, $f_{nd} \approx 1/(2\pi RC_{CM})$, with C_{CM} the capacitance at the output node of the DDA circuit ($C_{CM} \approx 2C_{gs7,8}$). Thus, the expression for the phase margin PM of the CMFB loop is approximately:

$$PM \approx 90º - arctg\left[\frac{GBW}{f_{nd}}\right] \tag{5.5}$$

$$PM \approx 90º - arctg\left[4g_{m1-4}g_{m7,8}\frac{C_{gs7,8}}{C_L}R^2\right] \tag{5.6}$$

Hence, the choice of *R* creates a tradeoff between DC gain and GBW of the CMFB loop and the stability [6]. Assuming that a PM larger than 60º is necessary to ensure stability, the maximum value of *R* can be calculated.

$$R_{MAX} \approx \sqrt{\frac{\sqrt{3}C_L}{12g_{m1-4}g_{m7,8}C_{gs7,8}}} \tag{5.7}$$

Another advantage of the LCMFB scheme is that the complementary AC signal variations at the drains of M_5 and M_6 leads to a virtual ground at their common gate, so that the parasitic capacitances at this node have no influence.

The three CMFB circuits of Figure 5.2 have been simulated using a 0.5 µm n-well technology, whose nominal NMOS and PMOS threshold voltages are 0.64 V and -0.92 V, respectively. As for the FDA, a single-stage differential amplifier with active load was chosen. The values of the different components are included in Table 5.1.

Component	Value
M_1-M_4	40 µm/0.6 µm
M_5-M_8	60 µm/0.6 µm
R	30 kΩ

Table 5.1. Parameters of design

Bias current I_B was taken as 10 µA, supply voltages were set to ±1 V and the reference common-mode voltage was V_{CMref} = 0.2 V. As load, two grounded capacitors were employed.

Figure 5.3 displays the simulated open-loop frequency response of the CMFB loop. Conventional CMFB circuit has a DC gain of 19.01 dB and a phase margin of 95º. The alternative approach (Figure 5.2(b)) presents a DC gain of 54.63 dB (the highest one), but the worst phase margin (only 3º). As an intermediate case, the proposed CMFB circuit is the best solution, because its DC gain is 34.24 dB, increasing noticeably the DC gain of the conventional CMFB circuit, and phase margin is good (70º) comparing with Figure 5.2(b).

Besides, there is also an increase of the gain bandwidth product (12 MHz vs. 2.2MHz of the conventional version).

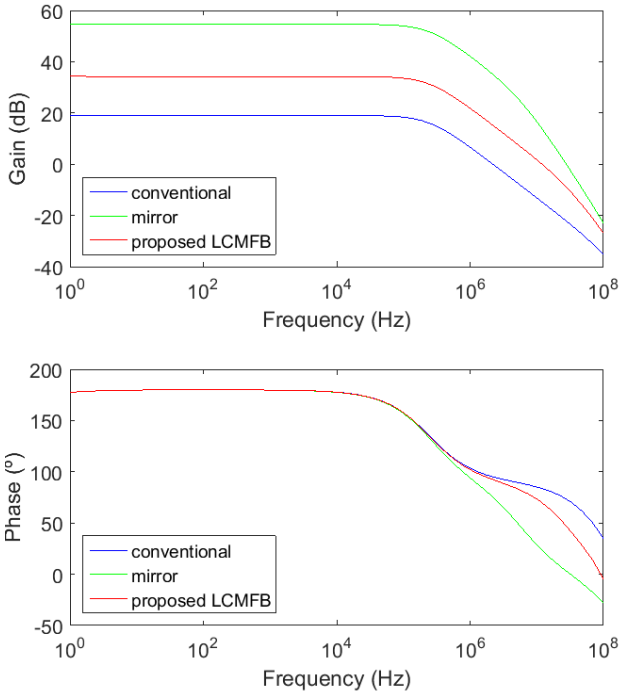


Figure 5.3. Simulated open-loop frequency response of the CMFBs

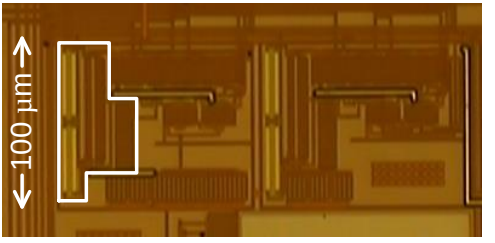


Figure 5.4. Microphotograph of the proposed DDA CMFB

A chip prototype was fabricated using the same 0.5 µm CMOS technology, including two single-stage differential amplifiers with active load, whose CM output voltage were controlled by the conventional and the proposed CMFB circuits. As CMFB in Figure 5.2(b) was unstable, it was not fabricated. Figure 5.4 displays a microphotograph of the manufactured chip. The white

square marks the proposed CMFB circuit, whose silicon area is approximately 0.003 mm^2.

Both amplifiers were connected in unity gain configuration in order to obtain their transient response. The nominal value of resistors R was 100 kΩ and they were fabricated on-chip. Bias currents and supply voltages were the same as for simulations. Two 47 pF external load capacitors were employed. If parasitic capacitances from the pad, board and test probe are considered, the total C_L was approximately 80 pF.

In the first place, the transient response of the amplifiers to sudden changes in the common-mode reference voltage was measured. With this purpose, a DC source was connected to the input nodes that sets the DC operating point correctly. A 100 kHz 0.2 V square wave was employed as V_{CMref}. Figure 5.5 shows these connections.

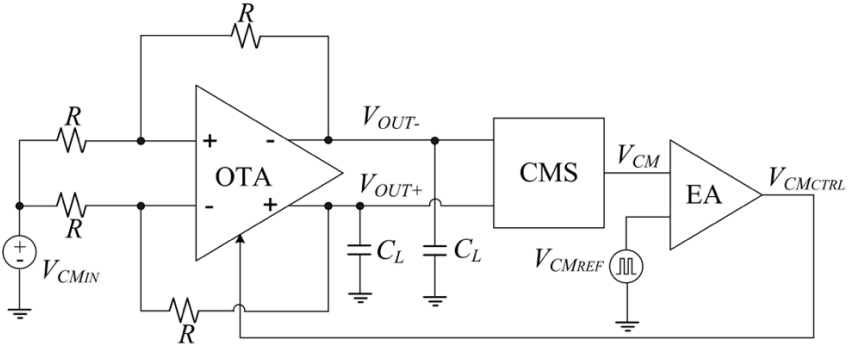


Figure 5.5. Circuit configuration used to measure the transient response for sudden changes in V_{CMREF}

The obtained results are drawn in Figure 5.6. Input voltage (V_{CMref}) is represented in green color, and blue and red lines are the output common-mode voltage of conventional and proposed CMFB circuit, respectively. As it can be seen, the proposed topology has a stable and faster settling.

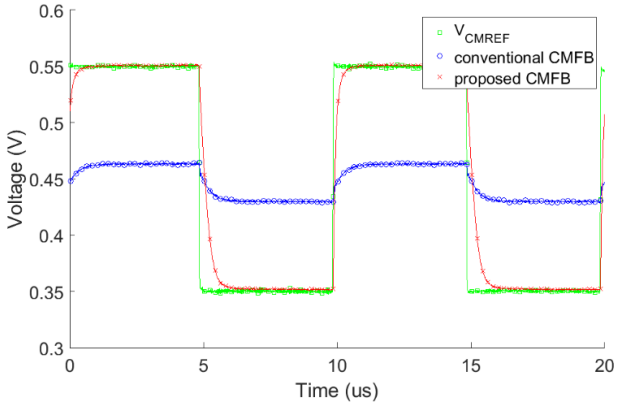


Figure 5.6. Measured transient response of conventional and proposed circuit

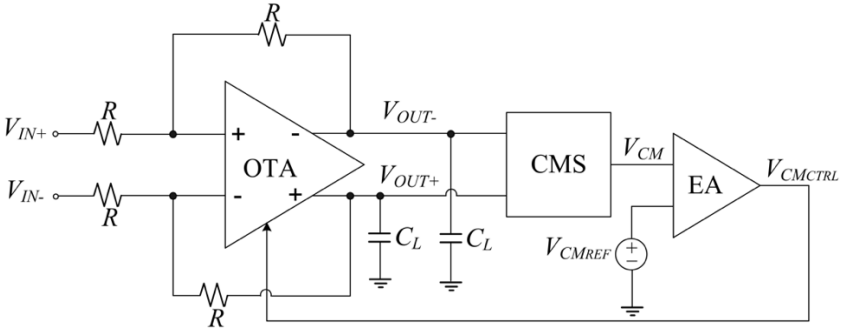


Figure 5.7. Circuit configuration to measure the transient response to a differential input signal

The measured positive and negative input and output signals are plot in Figure 5.8, as well as the input and output common-mode voltages, for both the conventional and proposed CMFB circuits. In order to obtain these measurements, topology in Figure 5.7 was employed, applying to V_{IN+} and V_{IN-} inverted squared signals. It can be seen that the proposed CMFB reaches an output common-mode voltage close to V_{CMref}, and shorter and smaller peaks are obtained at the transitions. However, the conventional one has an output common-mode voltage of 0.35 V, which is not an accurate value, as it should be around 0.5 V. Thus, the advantages of the proposed CMFB are experimentally evidenced, due to its improved accuracy and speed.

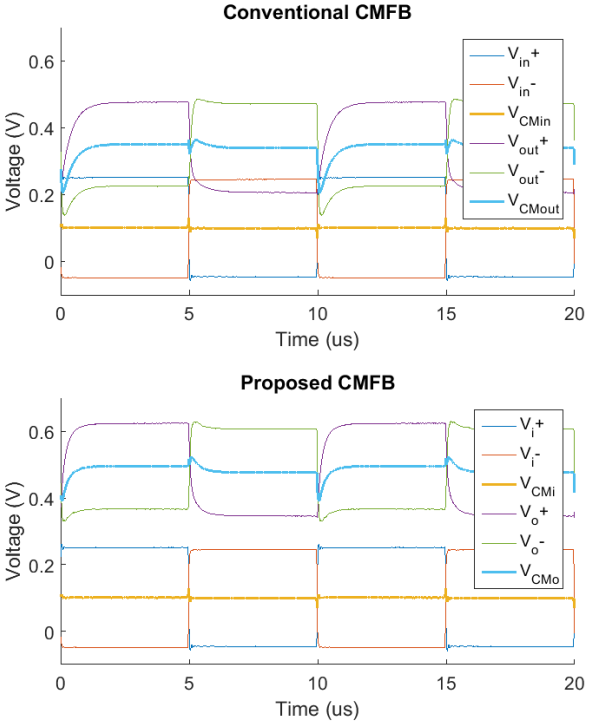


Figure 5.8. Measured transient response to a differential input signal (a) Conventional (b) Proposed

Accordingly, thanks to the inclusion of LCMFB techniques, it is proven that the proposed CMFB circuit has better features than the conventional one, improving A_{DC} in 15.23 dB and GBW by a factor 5.45 versus the conventional CMFB DDA circuit.

5.2 Power efficient class AB amplifier

The OTA Miller is one of the most commonly used amplifiers due to its simplicity. However, even if its fully differential version is adopted, its performance is often not enough for low voltage applications, due to its class A operation (its maximum output current is limited by its bias current I_B) and its limited transconductance (thus GBW).

In order to avoid these drawbacks, a new class AB fully differential amplifier is presented, which achieves a nearly ideal current efficiency (CE),

since the large dynamic output currents are directly generated at the output branches.

Figure 5.9(a) shows a conventional single-stage fully differential amplifier. It is a differential pair (M_8, M_9) biased by a constant current source $2I_B$ and with two current sources (M_3, M_6) as active loads. A common-mode feedback (CMFB) circuit, not shown, senses the output common-mode voltage and generates the voltage $V_{CM_{ctrl}}$ that controls the current sources M_4, M_5 to set such common-mode output voltage to the desired value. Without loss of generality, M_4, M_5 were designed to drive the same current $I_B/2$ as M_3 and M_6. The DC gain A_{DC}, gain-bandwidth product GBW and slew rate (SR) are

$$A_{DC} = g_{m8,9} \cdot R_{out} = g_{m8,9} \cdot \left(r_{o8,9} \| r_{o3,6} \| r_{o4,5}\right) \tag{5.8}$$

$$GBW = \frac{g_{m8,9}}{2\pi C_L} \tag{5.9}$$

$$SR = \frac{2I_B}{C_L} \tag{5.10}$$

Note that an increase in the static power is required in order to enlarge the SR, since the maximum output current is $2I_B$.

The circuit proposed is shown in Figure 5.9(b). The constant bias current source has been replaced by an adaptive biasing stage [7]. Transistors M_{10}-M_{11} are matched to M_8-M_9, enforcing well-controlled quiescent currents in the differential pair transistors. When a non-zero differential input $V_{id} = V_{in+} - V_{in-}$ is applied, the flipped voltage followers M_{10}-M_{12} and M_{11}-M_{13} allow increasing the V_{GS} of M_8 by V_{id} and decreasing the V_{GS} of M_9 by $-V_{id}$. This way, the full differential input signal is applied to each differential pair transistor, increasing gain by 2 compared with Figure 5.9(a). Moreover, for large positive V_{id}, a large current not bounded by I_B is supplied by M_{13} and a current smaller than I_B is supplied by M_{12}, increasing the positive SR. Similarly, for large negative V_{id} a large current is supplied by M_{12}, and the current generated by M_{13} is decreased, increasing the negative SR.

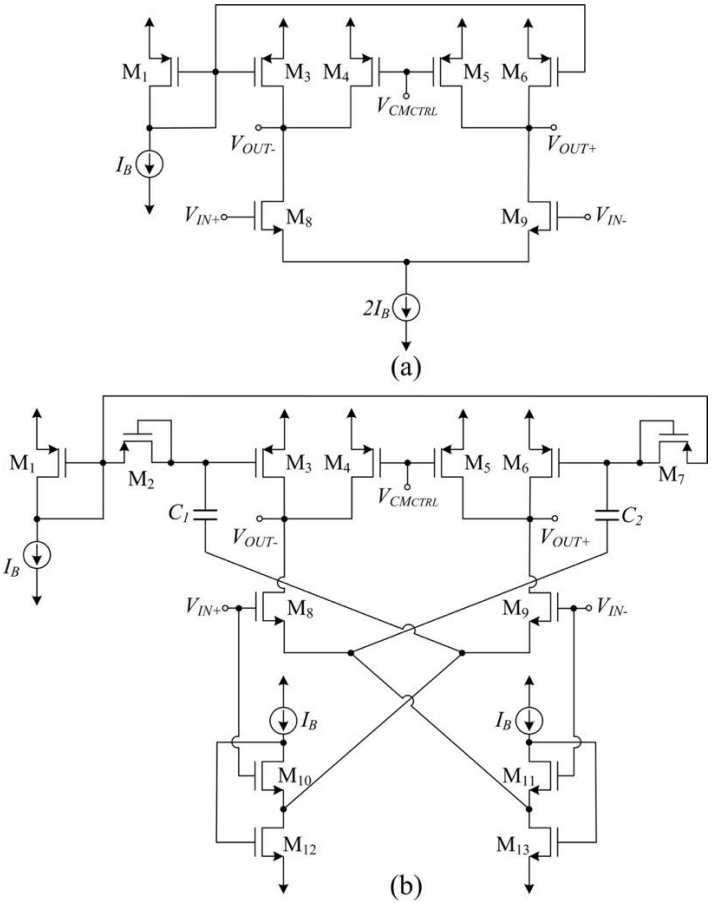


Figure 5.9. Single-stage differential amplifiers (a) Conventional class A amplifier (b) Proposed class AB amplifier with adaptive biasing

To further increase SR and GBW, current sources M_3 and M_6 in Figure 5.9(b) are also adaptively biased using quasi-floating gate (QFG) techniques [8]. Transistors M_2 and M_7 act as pseudo resistors with very large resistance R_{large}. Thus, capacitors C_1 and C_2 cannot discharge rapidly so that they act as DC level shifters that translate input signal variations to the gates of M_3 and M_6, respectively. The voltage followers M_{10}-M_{12} and M_{11}-M_{13} are re-used to drive C_1 and C_2, avoiding loading of the input terminals. For large positive V_{id}, C_1 forces a decrease in the gate voltage of M_3 and C_2 forces an increase in the gate voltage of M_6. Hence, the current in M_6 decreases and the current in M_3 increases, further increasing the positive SR versus the amplifier of

Figure 5.9(a). Similarly, negative SR is increased by the reduction of the current in M_3 and the increase of current in M_6 for large negative V_{id}.

Expressions for A_{DC} and GBW in the amplifier of Figure 5.9(b) are

$$A_{DC} = (2g_{m8,9} + \alpha g_{m3,6}) \cdot R_{out} = (2g_{m8,9} + \alpha g_{m3,6}) \cdot (r_{o8,9} \| r_{o3,6} \| r_{o4,5}) \quad (5.11)$$

$$GBW = \frac{2g_{m8,9} + \alpha g_{m3,6}}{2\pi C_L} \quad (5.12)$$

The factor 2 of $g_{m8,9}$ is caused by adaptive biasing of the differential pair, and the extra term $\alpha g_{m3,6}$ is due to the signal injected at the gate of M_3 and M_6 by C_1 and C_2, with $\alpha \approx C_{1,2}/(C_{1,2} + C_{gs3,6})$ the attenuation from the inputs to the gates of $M_{3,6}$. Hence, M_3 and M_6 are no longer simple current sources but they contribute to the amplifier's transconductance.

A test chip prototype with both amplifiers of Figure 5.9 was fabricated in a 0.5 µm CMOS process. The class AB CMFB circuit explained in Section 5.1 was employed for both amplifiers, in order to achieve fast CMFB operation with low-power consumption. Poly–poly capacitors C_1 and C_2 were used with a nominal value of 1 pF. Transistor aspect ratios are included in Table 5.2. A microphotograph of the amplifier of Figure 5.9(b) is shown inside the white box of Figure 5.10. The silicon area employed is 130 µm × 100 µm.

Transistor	**W/L** (µm/ µm)
M_1, M_3-M_6	60 / 0.6
M_2, M_7	1.5 / 1.05
M_8, M_9	40 / 0.6
M_{10}, M_{11}	20 / 0.6
M_{12}, M_{13}	40 / 1.05

Table 5.2. Aspect ratio of transistors of Figure 5.X

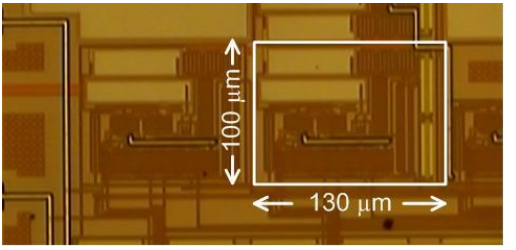


Figure 5.10. Microphotograph of the class AB amplifier of Figure 5.9(b)

Measurements were done using the amplifiers as voltage followers as explained in Appendix A (see Figure 5.7), where four matched 100 kΩ on-chip resistors are employed. Supply voltage was ±1 V. The output common mode voltage was set to 0.2 V. Two external grounded load capacitors of 47 pF each were employed, which added to the pad, board and test probe parasitic capacitances lead to a $C_L \approx 70$ pF. The measured response of the amplifiers is shown in Figure 5.11. A 100 kHz 0.55 V input square wave was used. Note the SR improvement achieved.

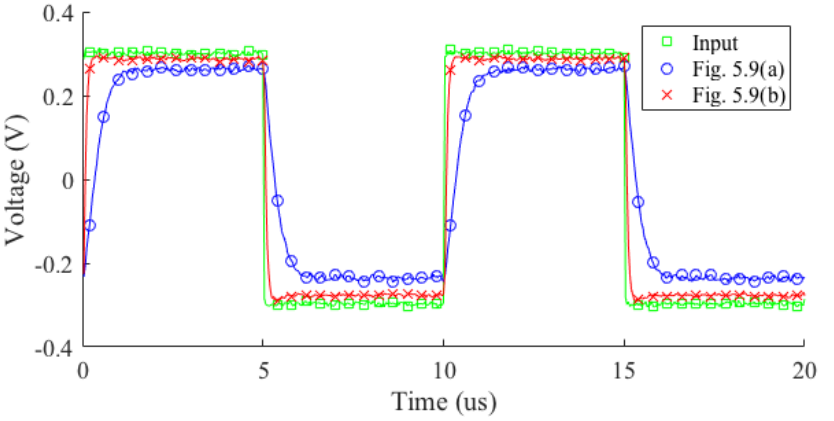


Figure 5.11. Transient response of amplifiers in Figure 5.9

Table 5.5 summarizes the main performance parameters of the two amplifiers of Figure 5.9. Note that the proposed amplifier improves dynamic performance and GBW maintaining similar noise level, and without degrading phase margin. In addition, a comparison with other class AB amplifiers is included in Section 5.6, using the two figures of merit (FoM) defined in Chapter 4.

Hence, a class AB version of the conventional one-stage fully differential amplifier has been presented, based on QFG and adaptive biasing techniques. The circuit improves both large and small-signal performance, maintaining supply voltage requirements and quiescent currents. The achieved CE is nearly ideal due to the absence of internal replication of the large dynamic currents delivered to the load.

5.3 Super class AB OTA

As it was said previously, operational transconductance amplifiers (OTA) are widely used in several applications. In order to achieve fast settling response, they should present good performance, especially in terms of slew-rate (SR) and gain-bandwidth product (GBW). Class AB operation is a must if low power is required to avoid the constraint in output current caused by I_B. As it was explained in Chapter 2, there are different approaches when designing class AB OTAs: boosting the bias current of the differential input pair for high input swings (with adaptive biasing techniques), boosting the current in the active load of the input stage (e.g. with LCMFB) or both, obtaining a Super Class AB OTA. Super Class AB OTAs [6] are characterized by boosting the output current proportionally to V_{id}^4 instead of V_{id}^2 (as usual for class AB OTAs), with V_{id} the differential voltage at the input. Hence, they achieve very high Slew Rate. However, the fully differential version of Super Class AB OTAs does not fully exploit the dynamic improvement achievable as the output branches are biased by conventional current sources.

A new fully differential Super Class AB OTA is proposed in this thesis which solves this issue. Introducing minor changes on a class AB OTA, slew rate is increased noticeably. Besides, small-signal performance is also improved without sacrificing static power consumption. This proposed Super Class AB amplifier is based on three different techniques: adaptive biasing techniques at the input pair (explained in Section 2.2.3.1), local common-mode feedback at the active load (Section 2.2.3.2), and finally, the use of Quasi-Floating Gate transistors (Section 2.1.2) in order to adaptively bias the output current sources.

Figure 5.12 shows the conventional class A fully differential current mirror OTA (Figure 5.12(a)), a Super Class AB OTA (Figure 5.12(b)) [6] and the proposed Super Class AB QFG OTA (Figure 5.12(c)). The constant differential pair bias current source $2I_B$ of Figure 5.12(a) is replaced in Figure 5.12(b) and Figure 5.12(c) by an adaptive biasing circuit which provides very small quiescent currents to M_1 and M_2 [16] [17]. When such adaptive circuit senses a large differential input, it automatically boosts the bias current provided. In addition, in Figure 5.12(b) and Figure 5.12(c), LCMFB [5] has been used. Finally, in Figure 5.12(c), the QFG technique [18] is used to dynamically bias the output current sources.

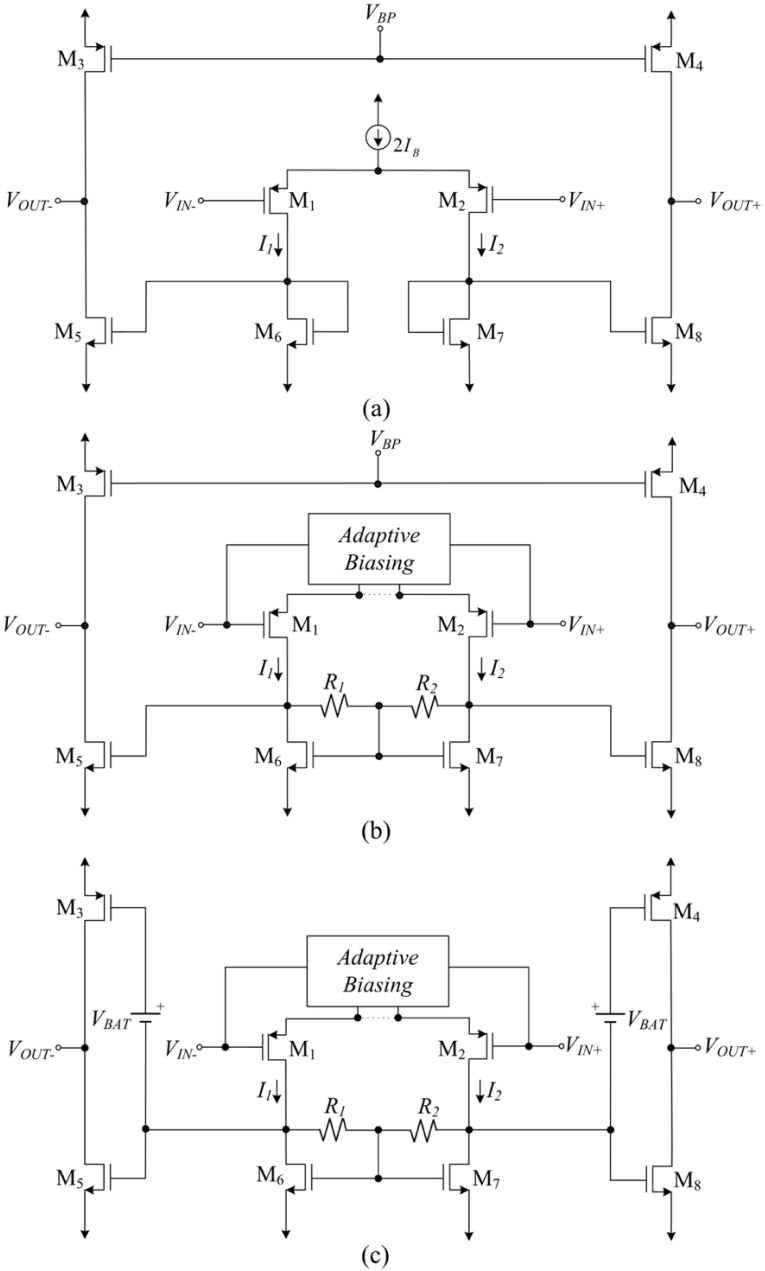


Figure 5.12. Fully Differential Amplifiers (a) Class A (b) Super Class AB (c) Proposed Super Class AB QFG

In order to adaptively bias the input pair, the topology shown in Figure 2.20 has been adopted. With this change, currents larger than I_B are obtained when a differential input signal is applied, as expressed in Equations 2.26 and 2.27. In addition, small signal transconductance is doubled, caused by the enhancement in small signal differential current (Equation 2.28).

Besides, the active load is also improved by using Local Common-Mode Feedback scheme (Figure 2.23(b)). By adding two resistors between the drains of transistors M_6 and M_7, under dynamic conditions, output currents are boosted proportionally to V_{id}^4, obtaining a Super Class AB amplifier. Apart from that, also the GBW is improved, as described by:

$$GBW = \frac{2g_{m1,2}g_{m5,8}R_{X,Y}}{2\pi C_L} \tag{5.13}$$

with $R_{X,Y} \approx R_{1,2}||r_{o6,7}||r_{o1,2}$. Thus, the increase factor versus circuit in Figure 5.12(a) is $2 \cdot g_{m5,8} \cdot R_{X,Y}$.

Finally, transistors M_5 and M_8 has been replaced by QFGMOS transistors with the objective of adaptively biasing the output branch. The topology shown in Figure 2.6(b) has been adopted. This way, an extra path for the input is added, increasing the transconductance of the amplifier, hence enhancing the GBW of the OTA in Figure 5.12(c), being this parameter:

$$GBW = \frac{2g_{m1,2}(g_{m5,8}+\alpha g_{m3,4})R_{X,Y}}{2\pi C_L} \tag{5.14}$$

The detailed schematic of the proposed super class AB QFG OTA is presented in Figure 5.13, based on the previous techniques. Additional current sources M_9 and M_{10} are used in the output branch to set the common-mode voltage at the output. In this way, in quiescent conditions, output branch currents are $I_B + I_B$', where I_B' is the current driven by transistors M_9 and M_{10}. Instead of using two additional PMOS current source transistors in order to inject I_B', M_3 and M_4 have been resized to provide this additional current. Because of the differential output topology, a CMFB circuit is needed. The previously explained CMFB circuit, shown in Figure 5.2(c), has been used.

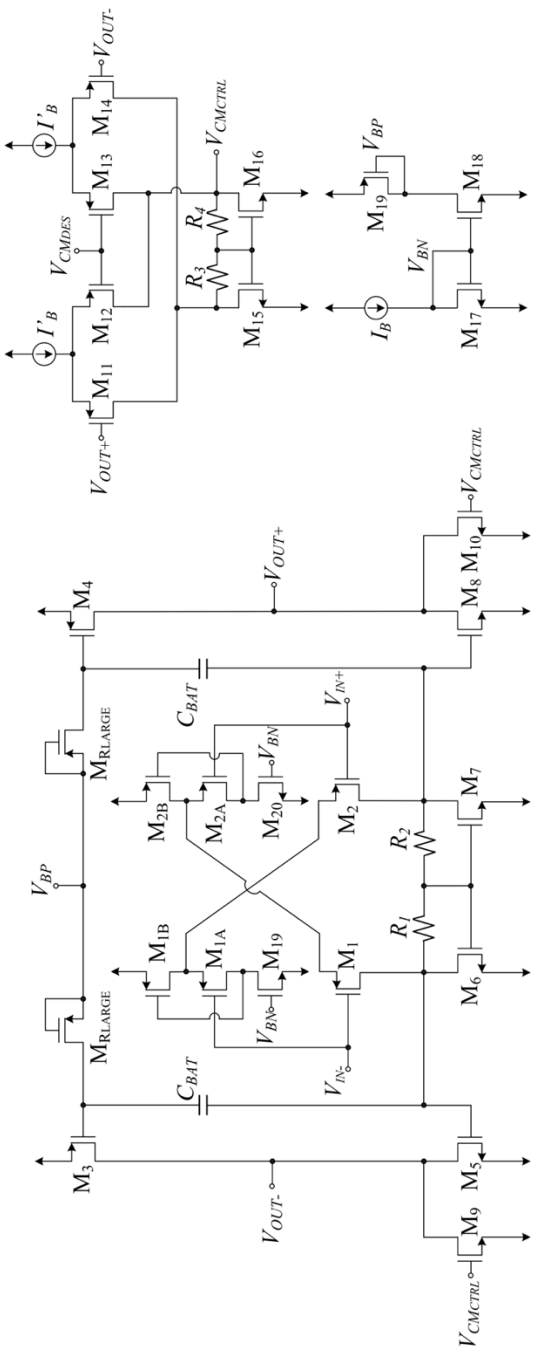


Figure 5.13. Proposed class AB QFG OTA with improved CMFB circuit

The three OTAs in Figure 5.12(a), Figure 5.12(b) and Figure 5.13 have been simulated using the same 0.5 µm CMOS technology employed previously. The transistor sizes employed are shown in Table 5.3. Capacitors C_{BAT} have a value of 1 pF.

Transistor	**W/L** (µm/µm)
M_1-M_2	50/0.6
M_{1A}-M_{1B}	50/0.6
M_{2A}-M_{2B}	240/0.6
M_3-M_4	180/0.6
M_5-M_{10}	60/0.6
M_{11}-M_{14}	50/0.6
M_{15}-M_{16}	60/0.6
M_{R1}-M_{R2}	1.5/0.6

Table 5.3. Transistors size of the Super Class AB QFG OTA

A dual supply voltage of ±1 V was applied, and the bias current I_B was 10 µA. The bias current of CMFB circuit, I_B', was 10 µA too. This current could be smaller to decrease the power consumption. The OTAs were connected in unity gain negative feedback shown in Figure 5.7 for time-domain simulations.

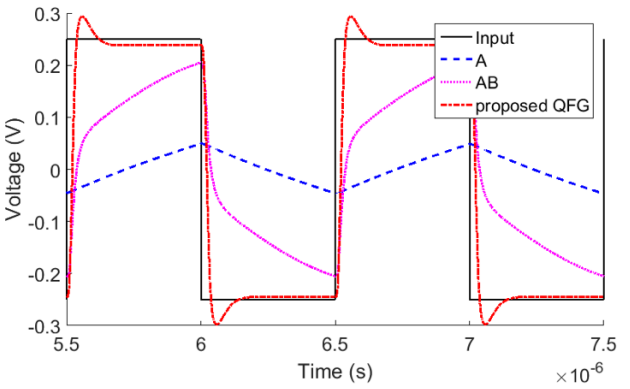


Figure 5.14. Simulated transient response of the OTAs

The input signal was a 1 MHz 0.5 V square wave with a -0.5 V common-mode voltage. The resistor R shown in Figure 5.7 had a nominal value of 100 kΩ. A high load capacitance of 70 pF is used to demonstrate the high current driving capability of the proposed OTA. The simulated output of the

OTAs is plotted in Figure 5.14. Note the stable and faster settling of the class AB QFG OTA proposed.

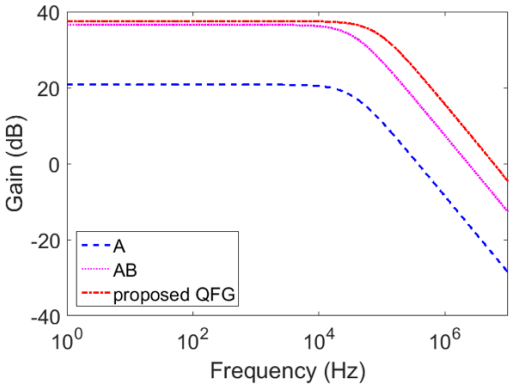


Figure 5.15. Simulated open-loop frequency response of the OTAs

Figure 5.15 shows the simulated open-loop magnitude response of the OTAs. The DC gain increases by 16.5 dB versus the class A OTA of Figure 5.12(a) and almost 1 dB compared to the class AB OTA shown in Figure 5.12(b). Concerning the increase in GBW, it is approximately a factor 16 due to the improved transconductance provided by the use of QFG transistors and the enhaced bandwidth of the proposed CMFB scheme provides.

Table 5.5 indicates relevant performance parameters of the OTAs. The slew rate is increased approximately 86 times for the same quiescent current and load capacitance. The settling time in the proposed OTA is 36 ns, while the classic class A OTA cannot settle for this input signal and load. Simulated THD is <1% for a 0.9 V_{pp} input sinusoid, whereas the conventional class A OTA shows THD>2% due to settling limitations.. The dynamic range of the proposed OTA is higher than for class A and class AB OTAs, despite of integrating its equivalent input noise density in a greater frequency band (corresponding to their GBW product). However, static power increases a 20% by the extra bias current required. This issue can be solved if a smaller bias current of CMFB circuit, I_B', is used. Another drawback is that the silicon area is higher due to the floating capacitors C_{BAT} and the resistors used in the LCMFB technique.

A test chip was fabricated using the same 0.5 μm CMOS technology, and containing the circuit of Figure 5.13 connected following the topology of Figure 5.7. Resistors R were fabricated on chip, while capacitors C_L were external. A photograph of the fabricated OTA is shown inside the white box of

Figure 5.16. The silicon area employed for the circuit is approximately 0.045 mm^2.

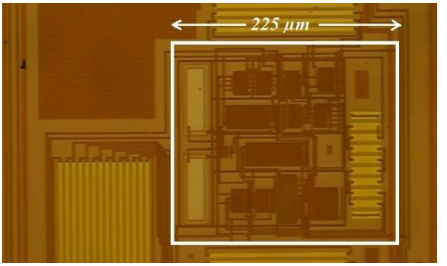


Figure 5.16. Microphotograph of the proposed super class AB QFG OTA

The measured response of the proposed OTA to a 100 kHz 0.5 V square input waveform is plotted in Figure 5.17. Bias current I_B was 30 μA. A load capacitance of 47 pF was employed, which is increased to about 70 pF by the pad, board and test probe parasitic capacitances. Measured positive and negative SR values are 11.8 V/μs and -11.2 V/μs respectively, and the measured settling time is 60 ns. The measured THD for an input tone of 100 kHz and 0.9 V_{pp} is -53.44 dB.

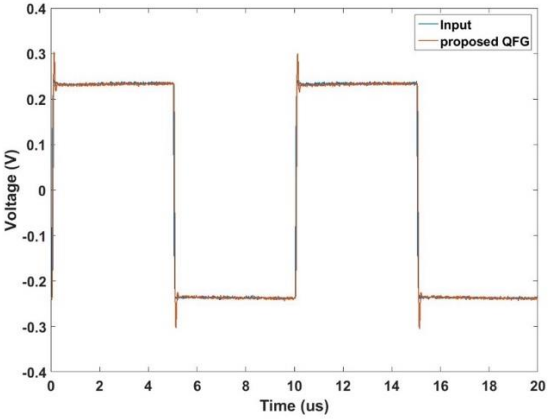


Figure 5.17. Experimental transient response of the proposed OTA

Therefore, thanks to diverse adaptive biasing techniques, an improved class AB QFG OTA has been proposed. This amplifier has a simple and compact implementation and does not require extra supply voltage. It also improves slew rate and settling significantly without increasing quiescent power. This circuit can be applied in micropower switched capacitor systems and in voltage followers requiring to drive large capacitive loads.

5.4 Class AB OTA with improved current follower

In Chapter 2, several cascode topologies have been proposed, which are very useful to improve the gain of the amplifier without adding extra gain stages, thus complicating stability and increasing power consumption. However, the signal swing available at the output is limited by the input transistors. This issue can be solved by avoiding to place the input transistors at the output branch. An efficient way of achieving that is the use of a current follower CF (or current amplifier CA if current gain K is provided) which conveys (and scales for $K \neq 1$) the signal current generated at the differential pair to the output branch, just as it was done in Section 5.3. Figure 5.18(a) shows the conceptual scheme. The CF/CA presents low impedance input (ideally a signal ground) in order to sense the input current without adding low-frequency poles or zeros, and also high- impedance output to achieve large amplifier gain.

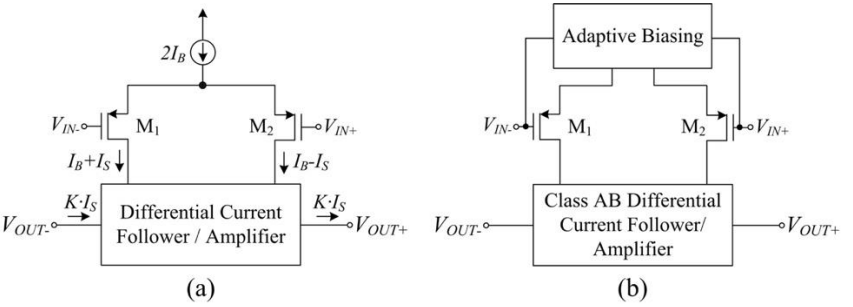


Figure 5.18. (a) Conventional single-stage class A amplifier
(b) Proposed single-stage class AB amplifier

Figure 5.19(a) and Figure 5.19(b) show two common implementations of these blocks, using current mirrors and common-gate amplifiers, respectively. The common-mode feedback (CMFB) circuit is not shown for simplicity. When they are applied to the circuit of Figure 5.18(a), the conventional current mirror (CM) amplifier and folded cascode (FC) amplifier result. The CM and FC amplifiers not only keep the gain and bandwidth of the telescopic cascode amplifier but also improve the output range. Note that in these arrangements the differential pair already provides an input bias current I_B to the CF/CA, so the bottom current sources in Figure 5.19(b) are $2I_B$.

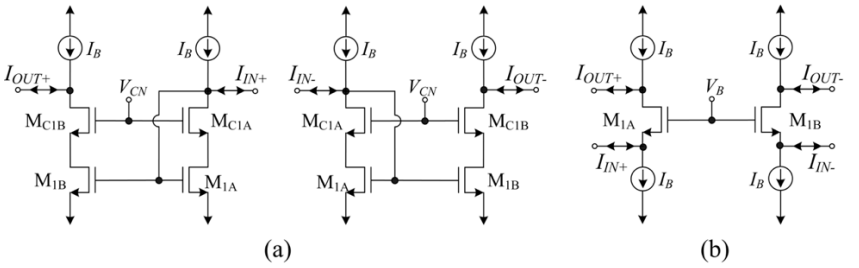


Figure 5.19. Differential CF implementation (a) with current mirrors (b) with common-gate transistors

A disadvantage of the topology of Figure 5.18(a) is that it operates in class A, limiting the output currents to the bias current $2I_B$. Hence, the power consumption must be increased in order to improve the dynamic performance of the amplifier. This can be solved by applying adaptive biasing techniques to the differential pair. With this method, class AB operation is achieved, as low quiescent currents can be used in the differential pair and at the same time large dynamic currents not bounded by the quiescent currents are generated for large input signals. As mentioned in previous sections, several class AB amplifiers have been reported, using different adaptive biasing techniques [6]-[15]. However, the CF/CA is often unchanged, which may limit the dynamic performance of the amplifier. The objective of this section is to design such CF/CA topologies in an optimal way to achieve class AB amplifiers. Besides, a novel class AB amplifier is presented as an application example.

Figure 5.19(a) shows two current mirrors, which is the most commonly used configuration for achieving a current follower or a current. They are frequently employed in OTAs, linear transconductors, CFOAs, current conveyors and several current-mode circuits. The main benefits of the current mirror are its simplicity and the possibility to scale the output current by the current mirror ratio K, thus improving the gain-bandwidth product (GBW) of the amplifier by the same scale factor K. However, there are also disadvantages using current mirrors. The main ones are:

a) The current mirror introduces a pole $\omega_p \approx -g_{m1B}/(C_{gs1A}+C_{gs1B})$ and a zero $\omega_Z \approx -(1+K)\cdot\omega_p$, which may limit high-frequency performance, mainly for large K ratios since they increase parasitic capacitance C_{gs1B}. This fact limits the maximum K value used in practice.

b) Increasing *K* also rises quiescent power consumption since *K* applies both to the quiescent current and the signal current.

c) Accuracy of the current mirror relies on perfect matching between the current mirror transistors, which is not possible in practice due to geometric and parametric variations.

The current follower of Figure 5.19(b) does not have any matching requirement between devices. The output current is exactly the inverted input current as long as the bias current sources in Figure 5.19(b) remain signal-independent. Moreover, the additional pole introduced is $\omega_p \approx -g_{m1}/C_{gs1}$, which is in general at higher frequency than that of Figure 5.19(a) for the same transistor dimensions and bias current, due to the lower intrinsic capacitance at the input. However, this CF cannot scale the output current, so it does not contribute to increasing the transconductance (and hence the GBW) of the amplifier.

A shortcoming of both circuits in Figure 5.19 is that the maximum signal current is limited by the bias current I_B. For the NMOS topology in Figure 5.19(a) the maximum current leaving the current mirror is I_B (a PMOS current mirror would lead to the same limitation for the current entering the mirror). In the current follower of Figure 5.19(b), the maximum signal current entering the circuit is I_B. In the next paragraphs, a modification is employed to overcome this limitation, yielding a class AB topology.

The proposed single-stage class AB amplifier corresponds to the topology shown in Figure 5.18(b). There are several choices for the adaptive biasing of the differential pair, as it was explained in Section 2.2.3.1 [6]. In this design, the cross-coupled DC level shifters option has been used, doubling the transconductance.

The differential CF/CA employed is shown in Figure 5.20. It is based on the differential high-swing current mirror implementation of Figure 5.19(a), including two modifications. First, the input current is sensed at the source of M_{CN1}-M_{CN2}, in order to benefit from the reduced input resistance at this node due to the FVF feedback loop. Second, the quasi-floating gate (QFG) technique [18] is applied to achieve class AB operation. It is based on including two capacitors C_{BAT} and two high-resistance pseudo-resistors M_{PR}. In quiescent

operation these new devices have no effect since capacitors act as open circuits and there is no current flowing through transistors M_{PR}. However, when a positive differential input current $I_{INd}=I_{IN+}-I_{IN-}$ appears, voltage at node *A* increases and voltage at node *B* decreases. Due to the large value of the equivalent resistance R_{large} of the pseudo resistors M_{PR}, capacitors C_{BAT} cannot discharge rapidly so that they behave as floating batteries, transferring voltage variations from nodes *A* and *B* to nodes *C* and *D*, respectively. The increased voltage at node *C* reduces the current flowing through transistors M_{P1}-M_{P2} at the right-hand side, and the decreased voltage at node *D* boosts the current flowing through transistors M_{P1}-M_{P2} at the left-hand side above I_B When a negative differential input current $I_{INd}=I_{IN+}-I_{IN-}$ appears, now voltage at node *A* decreases and voltage at node *B* increases, yielding a decrease at node *C* and an increase at node *D*. Hence the opposite situation happens at the output terminals. Consequently, positive and negative input currents much larger than I_B can be applied to either input terminal without compromising dynamic performance.

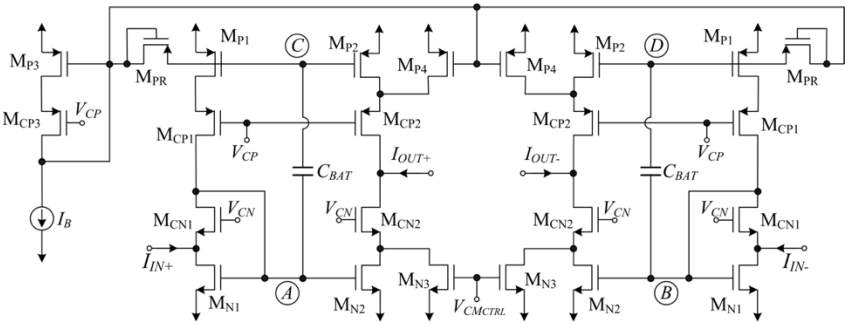


Figure 5.20. Class AB differential CF/CA using QFG techniques

The capacitive divider formed by C_{BAT} and the intrinsic capacitance C_P at the gate of M_{P1}-M_{P2} leads to attenuation in the voltage transfer from nodes *A* to *C* (and *B* to *D*) given by the expression $\alpha = C_{BAT}/(C_{BAT}+C_P)$. Moreover, the signal transferred to these nodes is also high-pass filtered by the first order *RC* filter formed by C_{BAT} and M_{PR}, with cutoff frequency $f_{-3dB}=1/[2\pi R_{large}(C_{BAT}+C_P)]$. Due to the extremely large value of R_{large} and the typically low value of C_P, a $f_{-3dB}<1$ Hz and $\alpha>0.75$ can be achieved with $C_{BAT}\approx 1$ pF. Hence in practice all the AC components of voltage at nodes *A* and *B* can be transferred to nodes *C* and *D* with low attenuation, with a modest increase in silicon area (about 1000 μm^2 more in the process employed).

The detailed circuit of the proposed class AB OTA of Figure 5.18(b) using the adaptive biasing mentioned and the CF/CA of Figure 5.20 is shown in Figure 5.21(a). A conventional CMFB circuit, based on a differential difference amplifier was used. It is shown in Figure 5.22.

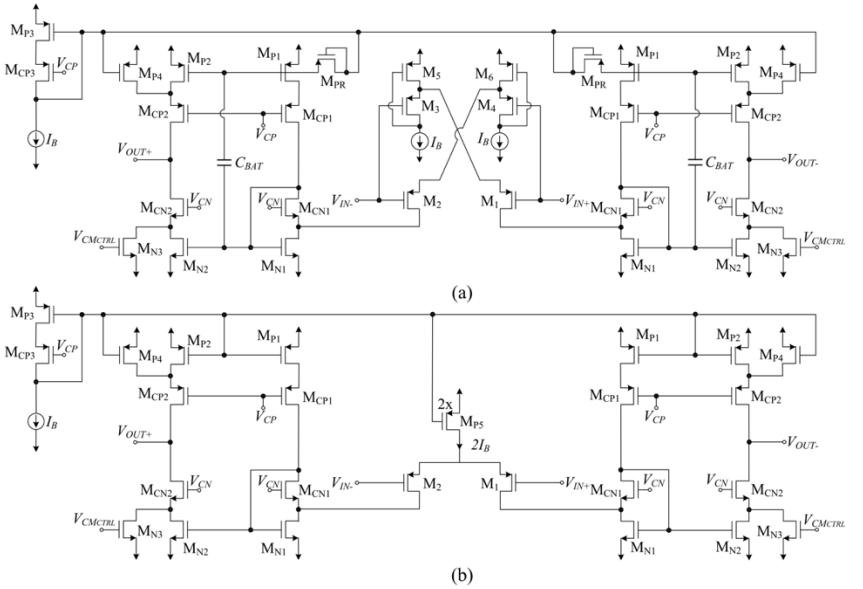


Figure 5.21. (a) Proposed class AB amplifier (b) Class A amplifier used for comparison

As for the small-signal parameters, the transconductance of the proposed amplifier is

$$G_{mAB} = 2Kg_{m1} \tag{5.15}$$

with K the current gain factor of the circuit in Figure 5.20, given by $K=(W/L)_{MN2}/(W/L)_{MN1}=(W/L)_{MP2}/(W/L)_{MP1}$. The output resistance of the amplifier is

$$R_{oAB} \approx g_{mCP2}r_{oCP2}(r_{oP2}\|r_{oP4})\|g_{mCN2}r_{oCN2}(r_{oN2}\|r_{oN3}) \tag{5.16}$$

and the DC gain is $A_{DC} = G_{mAB}\cdot R_{oAB}$. The GBW is given by

$$GBW_{AB} = \frac{Kg_{m1}}{\pi C_L} \tag{5.17}$$

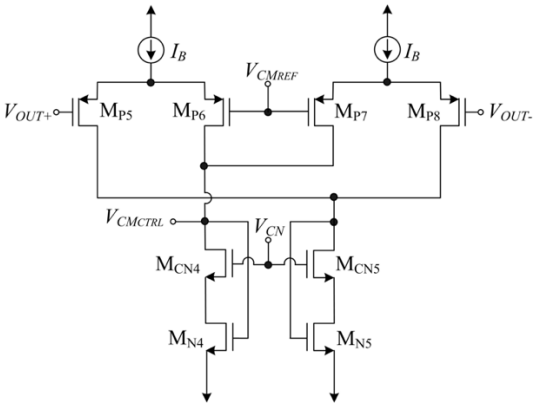


Figure 5.22. Common-mode feedback circuit

Besides small-signal analysis, an approximate expression for slew rate (SR) can be obtained by using the simple square law model for the MOS transistor in strong inversion and saturation. For a large positive differential input voltage V_{id}=V_{in+}-V_{in-}, current in transistor M_1 is

$$I_1 = \frac{\beta_1}{2}\left(\sqrt{\frac{2I_{BIAS}}{\beta_4}} + V_{id}\right)^2 \tag{5.18}$$

whereas current I_2 can be neglected. This large current is conveyed to the output by the circuit of Figure 5.20. Hence for a differential input step of A Volts, the SR_+ is

$$SR_{AB+} = \frac{K\beta_1}{2C_L}\left(\sqrt{\frac{2I_{BIAS}}{\beta_4}} + A\right)^2 \tag{5.19}$$

Analogously, for a large negative differential input step of amplitude A, the SR- is

$$SR_{AB-} = \frac{K\beta_2}{2C_L}\left(\sqrt{\frac{2I_{BIAS}}{\beta_3}} + A\right)^2 \tag{5.20}$$

In practice SR values are lower due to second-order effects not considered in the simple MOS square law model, and because some transistors can leave saturation for large transients.

Note that the SR for the class A version of Figure 5.21(b) using the same bias current is

$$SR_{A+} = SR_{A-} = \frac{2KI_{BIAS}}{C_L} \tag{5.21}$$

Considering thermal noise and assuming that all transistors operate in strong inversion and saturation, the equivalent input noise of the proposed amplifier is

$$\overline{v_{n,inAB}^2} = \frac{4k_BT\Delta f}{3g_{m1}^2} \times \left(g_{m1} + g_{m4} + g_{mN1} + g_{mP1} + \frac{g_{mP2}+g_{mP4}+g_{mN2}+g_{mN3}+g_{Mn4}}{K^2}\right) \quad (5.22)$$

Note that as expected the influence of the output branch transistors decreases for larger *K* when referred to the input. The CMFB circuit does not influence noise as its noise is cancelled by the differential output arrangement.

The class A and class AB amplifiers of Figure 5.21 were simulated using a 0.5 µm CMOS n-well process. A class A CF/CA (the circuit of Figure 5.20 but without capacitors C_{BAT} and pseudo-resistors M_{PR}) is used in the circuit of Figure 5.18 . The transistor sizes employed are shown in Table 5.4. Capacitors C_{BAT} have a value of 1 pF. Supply voltages were ±1 V, and bias currents I_B and I_{BIAS} were set to 10 µA. Cascode bias voltages V_{CP} and V_{CN} were set to -0.3 V and 0.2 V, respectively. Load capacitance was C_L = 25 pF.

Transistor	**W/L** (µm/µm)
M_1, M_2, M_3, M_4	100/1
M_5, M_6	100/0.6
M_{N1}, M_{N2}	60/1
M_{CN1}, M_{CN2}	60/0.6
M_{P1}, M_{P2}, M_{P3}, M_{P4}	100/0.6
M_{P5}, M_{P6}, M_{P7}, M_{P8}	200/0.6
M_{CP1}, M_{CP2}, M_{CP3}	200/0.6
M_{N3}, M_{N4}, M_{N5}, M_{CN4}, M_{CN5}	100/3
M_{PR}	1.5/1

Table 5.4. Transistor Aspect Ratio of amplifiers of Figure 5.21

Figure 5.23 shows the simulated open loop AC small signal response of both amplifiers of Figure 5.21. The DC gain of the class A and class AB amplifiers is 54.9 dB and 61.5 dB respectively. This improvement is mainly due to the extra 6 dB provided by the adaptive biasing topology. The GBW of the class A and class AB amplifiers is 1.07 MHz and 2.31 MHz, respectively. Note the increase in GBW by a factor >2. The phase margin of the class A and class AB amplifiers is 89.3º and 87º, respectively. At 2.31 MHz the phase margin of

the class A amplifier is 88º, hence a degradation of just 1º is observed for the class AB version.

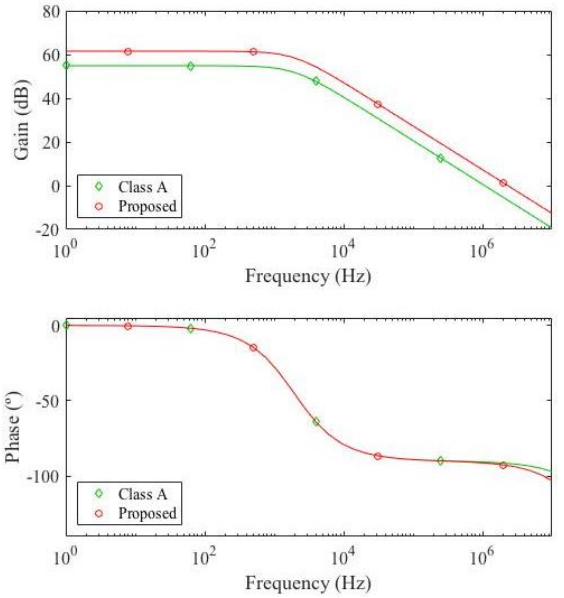


Figure 5.23. Simulated open-loop frequency response of amplifiers of Figure 5.18

The transient response of the amplifiers of Figure 5.21 were simulated connecting them in unity gain configuration using passive feedback resistors of R=100 kΩ, as shown in Figure 5.7, and the same C_L = 25 pF. A 100 kHz 0.4 V differential input square with -0.3 V common-mode voltage was applied to the input. Figure 5.24 shows the simulated output of the amplifiers. Note the stable and faster settling of the proposed class AB amplifier. The SR of the class A amplifier is 0.62 V/µs, while the SR of the proposed class AB amplifier is 2.7 V/µs, i.e., >4 times higher for the same quiescent current and load capacitance.

Figure 5.25 shows the simulated Total Harmonic Distortion (THD) using a 100 kHz differential input tone of different amplitude. Note the improved linearity of the proposed amplifier, due to the enhanced dynamic performance.

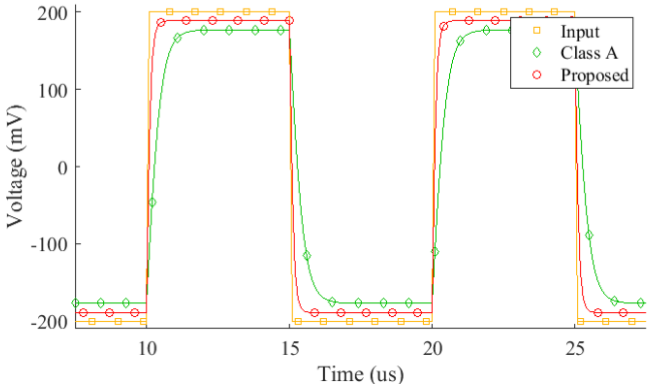


Figure 5.24. Simulated transient response of amplifiers of Figure 5.21

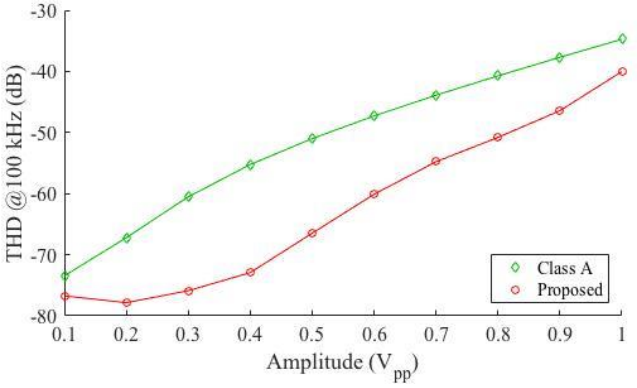


Figure 5.25. Simulated THD vs input amplitude at 100 kHz

The class AB amplifier of Figure 5.21(a) in the arrangement shown in Figure 5.7 was fabricated in the same 0.5 µm CMOS technology used for the simulations. On-chip resistors *R* were made by a high resistance polysilicon layer available in the technology. The outputs were directly connected to bonding pads. As no load capacitors were used off-chip, load capacitance in the measurements corresponds to the pad, board and test probe capacitance. Its estimated value is 25 pF. Figure 5.26 shows a microphotograph of the class AB amplifier, enclosed by the white rectangle. The silicon area employed is 500 µm × 150 µm. Supply voltage as well as bias currents/voltages employed for the measurements were the same as for the simulations.

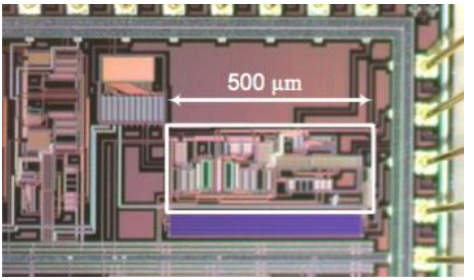


Figure 5.26. Microphotograph of amplifier in Figure 5.21(a)

Figure 5.27 shows the measured response to a 0.4 V 100 kHz periodic input square waveform. The measured SR is 3.4 V/µs, in close agreement with the simulation results.

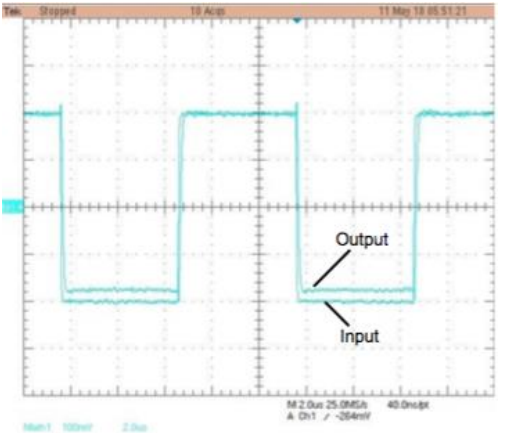


Figure 5.27. Measured transient response of amplifier in Figure 5.21(a)

Table 5.5 summarizes the main simulation and measurement results of the amplifier and other reported class AB amplifiers. The main drawback of the proposed amplifier is a small area increase due to the capacitors C_{BAT} and the adaptive biasing.

Hence, the combination of a power efficient adaptive biasing circuit and a class AB current follower able to handle the large dynamic currents generated is the main idea of the proposed amplifier. Simulation and measurement results confirm the advantages of this approach.

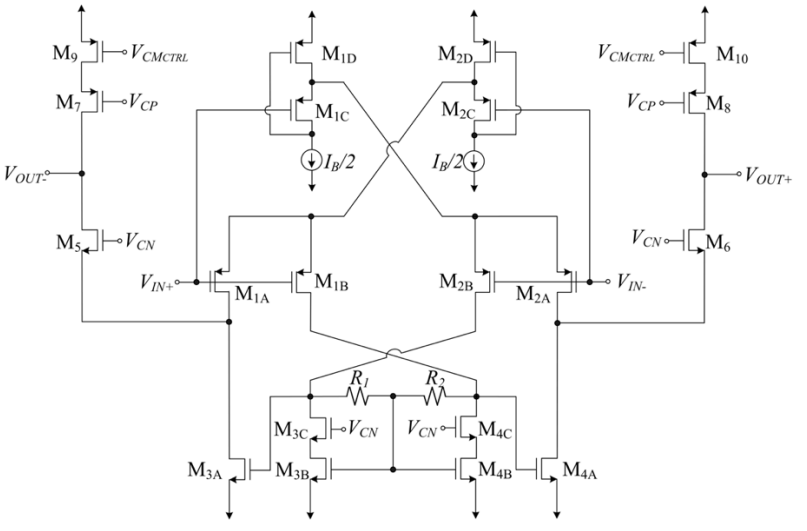
5.5 Differential class AB recycling folded cascode

In Chapter 4, several single-ended Recycling Folded Cascode topologies were proposed with good features. However, due to the multiple benefits of fully differential topologies previously explained in the introduction of this Chapter, even better performance can be obtained.

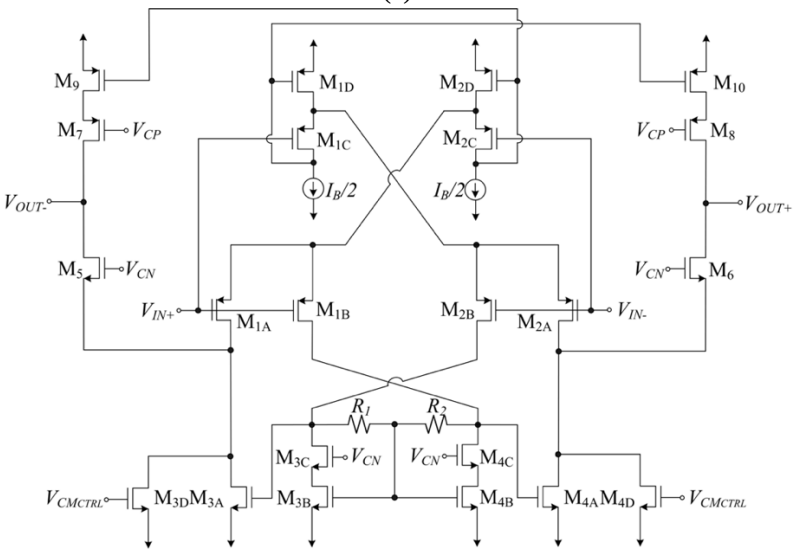
A fully differential (FD) version of the OTA of Figure 4.17 can be simply obtained by replacing the output current mirror by two matched current sources and including a Common-Mode Feedback (CMFB) circuit, as shown in Figure 5.28(a). The analysis performed for the single ended super class AB RFC OTA in Section 4.1.3 essentially applies to this FD implementation. However, as for the FD RFC OTA, there is a potential asymmetry in the charge/discharge rate of the outputs that can be balanced by a fast and accurate CMFB [14].

An alternative FD implementation is shown in Figure 5.28(b) based on [17]. The gates of M_9 and M_{10} are connected to the gates of M_{2D} and M_{1D}, respectively. Hence current in M_{1D} and M_{2D} is copied to the output branches, increasing the G_m and therefore the DC gain and GBW of the OTA.

Both the conventional (replacing the output PMOS current mirror by two matched current sources) and proposed fully differential implementation of the super class AB RFC OTA, shown in Figure 5.28, were simulated using a 0.5 μm CMOS technology. Time-domain simulations were done in closed-loop configuration. The same component dimensions, supply voltage and bias currents as for the single-ended versions were employed, that is, those in Table 4.4. The CFMB circuit of Figure 5.2(c) controlling NMOS current sources was used in both OTAs to get a fast CMFB loop. Table 5.5 summarizes the main results, evidencing the improvement of the OTA of Figure 5.28(b).



(a)



(b)

Figure 5.28. FD super class AB RFC OTA (a) Conventional (b) Proposed

Therefore, with the simple modification done in Figure 5.28(b), better performance is obtained: better linearity, greater GBW and DC gain (thus less input-referred noise) when comparing with Figure 5.28(a).

5.6 Comparison of the differential amplifiers

As in Chapter 4, a final Section is included in order to compare the amplifiers proposed in this Chapter, and also with other previously published ones.

Table 5.5 contains the most important parameters of every considered amplifier. Among the proposed ones, the OTA Figure 5.13 presents the highest Slew Rate value (18.1 V/μs). Its THD is also the lowest (since that of Figure 5.28(b) was calculated by simulation and with a lower amplitude). As for the small signal parameters, Figure 5.28(b) has the highest DC gain and GBW.

It is worth mentioning that some of the equivalent input noise values were obtained by simulation, thus those values are lower than the experimental ones.

To simplify the comparison of all the amplifiers, Figure 5.29 is provided. OTAs of Figure 5.13, Figure 5.28(a) and Figure 5.28(b) present the best FoMs in both small and large signal domains, even if compared with other previously published amplifiers which were fabricated in newer technologies.

Thus, it can be said that the fully-differential amplifiers proposed in this chapter obtain very good performance despite their low power consumption, i.e, they are power-efficient solutions.

	***CMOS tech.* (µm)**	**C_L (pF)**	***SR+* (V/µs)**	***SR-* (V/µs)**	***THD (dB)***	***A_{DC}* (dB)***	***PM* (º)***	***GBW (MHz)***	***Eq. input noise @1MHz (nV/√Hz)***	***Power* (µW)**	***Area* (mm²)**	***FoM_L***	***FoM_S***
Figure 5.9(a)	0.5	70	0.72	-0.85	-34.1 @100 kHz 0.6 V_{pp}	30.8	90	1	86	120	0.011	0.84	116.7
Figure 5.9(b)	0.5	70	6.3	-6.4	-53.9 @100 kHz 0.6 V_{pp}	36.7	89.8	2.35	84	160	0.013	5.51	205.6
Figure 5.12(a)	0.5	70	0.21	-0.21	-31.6 @100 kHz 0.9 V_{pp}	20.8	94	0.366	35.8*	200	0.024	0.15	25.6
Figure 5.12(b)	0.5	70	7.7	-7.6	-54.5 @100 kHz 0.9 V_{pp}	36.4	88.9	2.35	13.3*	240	0.040	4.49	137.1
Figure 5.13	0.5	70	18.1	-16.6	-71.7 @100 kHz 0.9 V_{pp}	37.3	80.5	6	12.4*	240	0.045	10.56	350
Figure 5.21(a)	0.5	25	3.4		-47 @100 kHz 0.5 V_{pp}	61.5	87	2.31	93	240	0.075	0.71	48.1
Figure 5.28(a)*	0.5	70	9	-9	-63 @100 kHz 0.5 V_{pp}	74.6	76	3	15*	140	--	9	300
Figure 5.28(b)*	0.5	70	9	-10	-72 @100 kHz 0.5 V_{pp}	76	74	4.1	14*	140	--	9.5	410

	CMOS process (µm)	C_L (pF)	*SR+* (V/µs)	*SR-* (V/µs)	*THD (dB)*	A_{DC}* *(dB)*	*PM** (º)	*GBW (MHz)*	*Eq. input noise @1MHz* (nV/√Hz)	*Power* (µW)	*Area* (mm^2)	FoM_L	FoM_S
[9]	0.13	>5.5	19.5	--	--	>70	>45	35	14.1	110	0.012	1.17	210
[10]	0.18	8	0.14	--	-52 @ 1 kHz 0.5 V_{pp}	51	60	0.057	--	1.2	0.057	0.75	30.4
[11]	0.18	20	2.89	--	-40 @0.4 V_{pp}	52	--	2.5	80	110	0.026	0.26	22.7
[12]	0.35	15	2.53	-1.37	--	88.3	66.1	11.67	<60	197	0.157	0.19	88.9
[13]	0.5	25	2.7	-3.3	-47.1 @ 2 V_{pp}	63.4	83	4.9	--	437.5	0.029	0.39	70
[14]	0.18	20	1.8	-3.8	-40.1 @250 kHz 0.4 V_{pp}	57.5	60	3	100	25.4	0.020	0.99	165.4
[15]	0.18	200	74.1	--	--	72	50	86.5	--	11900	0.070	2.24	261.7

**Simulation*

Table 5.5. Summary of measurement results and performance comparison

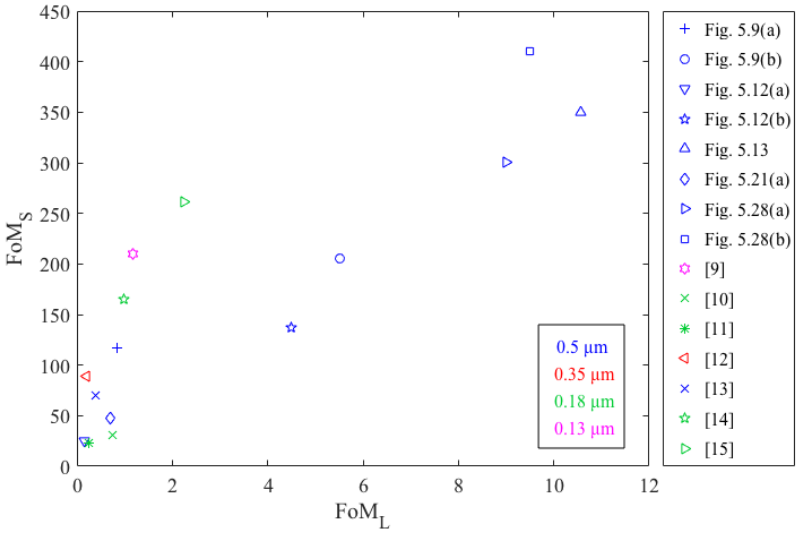


Figure 5.29. Comparative chart considering a small-signal and a large-signal FoMs

5.7 Conclusions

Chapter 5 proposes novel low-voltage class AB fully differential amplifiers, due to their several benefits versus single-ended topologies. Different techniques have been applied in order to develop these blocks whose performance has been improved compared with conventional circuits. In addition, an enhanced CMFB circuit has been proposed.

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Chapter 6

APPLICATIONS OF CLASS AB AMPLIFIERS

In Section 2.2.1, a low voltage technique was presented, based on choosing a more convenient DC operating point for the input transistors, achieving rail-to-rail operation. This technique can be applied to different systems, since the opamp is a very versatile analog building block.

In this Chapter, three different applications of the same technique are described. A low voltage buffer is proposed in Section 6.1. Section 6.2 describes a Sample and Hold. In Section 6.3, a Delta-Sigma modulator is presented, also capable of operating in low-voltage conditions. Finally, conclusions are given in Section 6.4.

Since two of these applications are related to Analog-to-Digital conversion, the main basic concepts of this process are introduced in Appendix D.

6.1 Low Voltage Buffer

In Chapter 2, different approaches have been presented in order to design low-voltage low-power amplifiers. However, there are more possible implementations. In [1], the concept of switched op-amps was proposed, which

made use of switched capacitors to achieve low-voltage op-amps. Based on this theory, in [2] the circuit shown in Figure 6.1 is proposed.

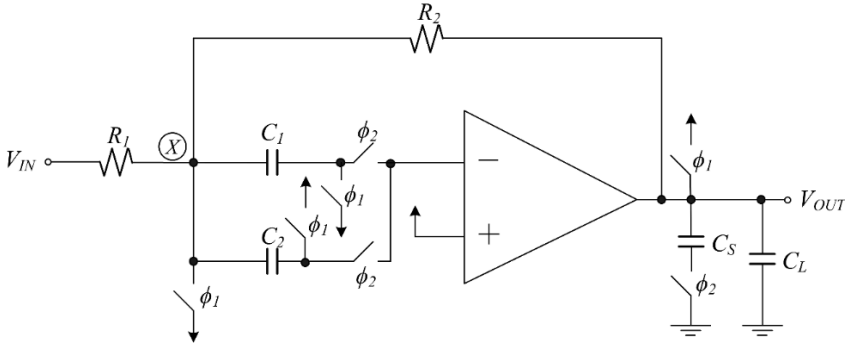

Figure 6.1. Switched op-amp buffer [2]

As it can be seen from the figure above, this amplifier is connected in inverting configuration. During phase ϕ_1, capacitor C_2 is charged to V_{DD}-V_{SS}, while charge in C_1 is null, as its terminals are connected to V_{SS}. However, in phase ϕ_2, both capacitors share their charge. As the positive input terminal of the amplifier is set to V_{DD}, the negative terminal is forced to the same voltage, thus voltage at node X is 0 V, which is the same voltage as the input common-mode voltage, permitting the amplifier to work in low-voltage operation.

The main drawback of this topology is that it only works in ϕ_2, as the output terminal is V_{DD} in ϕ_1. To solve this issue, the following circuit is proposed.

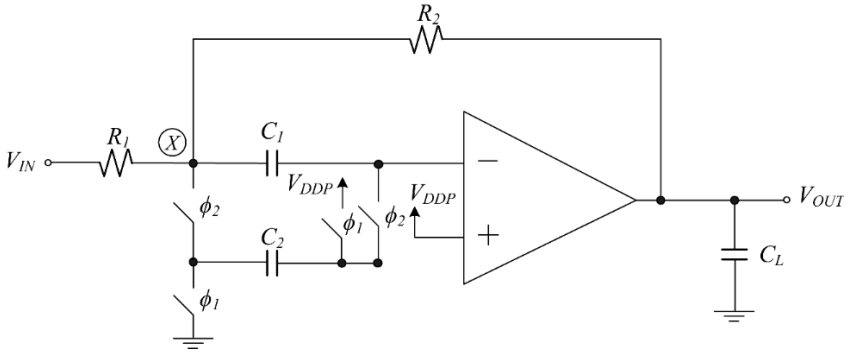

Figure 6.2. Proposed low-voltage amplifier

The proposed topology works as follows. In phase ϕ_1, C_2 is charged to V_{DDP}. (a voltage slightly lower than V_{DD}). Supposing C_1 is initially discharged,

in phase ϕ_2, C_1 and C_2 share their charge, thus node X is set to $V_{DDP}/2$. Phase ϕ_1 repeats, charging C_2 to V_{DDP}, and once again, in phase ϕ_2, both capacitors are connected in parallel, but this time, C_1 was charged to $V_{DDP}/2$, hence voltage node X becomes $V_{DDP}/4$. This process happens repetitively, making voltage at node X to decrease in each phase until it reaches 0 V. This implementation is only possible because C_1 is connected to the input terminal of the amplifier, which does not let any current flow through this terminal, hence C_1 does not lose its charge.

The proposed circuit not only can operate in low-voltage conditions with rail-to-rail input range, but also it works in both phases. This latter advantage implies a reduction of the slew rate requirements versus the circuit proposed in [2], as the output voltage does not reset its value to the positive supply voltage, and also makes this block suitable for continuous-time applications, despite using switched capacitors.

For comparative purposes, the proposed circuit is going to be compared with [2] and with the circuit in Figure 2.13, that was proposed in [3]. The amplifier block that is used in the three topologies is a two-stage OTA, formed by a conventional differential pair and a class AB QFG output stage with a compensation network built by compensation resistor R_C and capacitor C_C. It is shown in Figure 6.3.

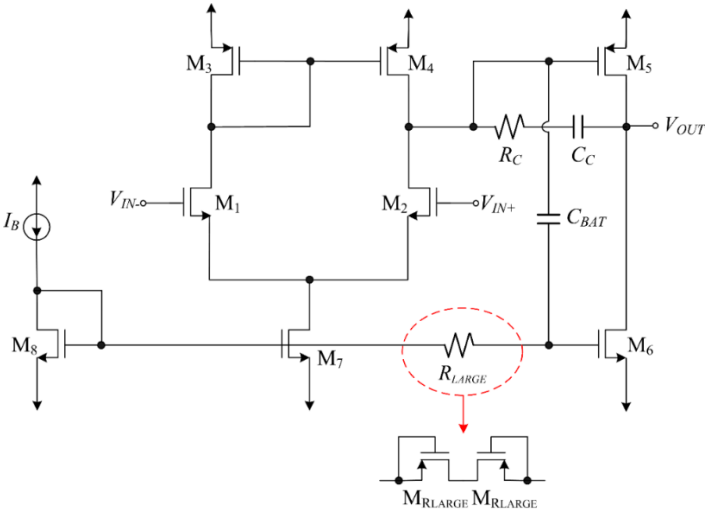

Figure 6.3. Two-stage OTA

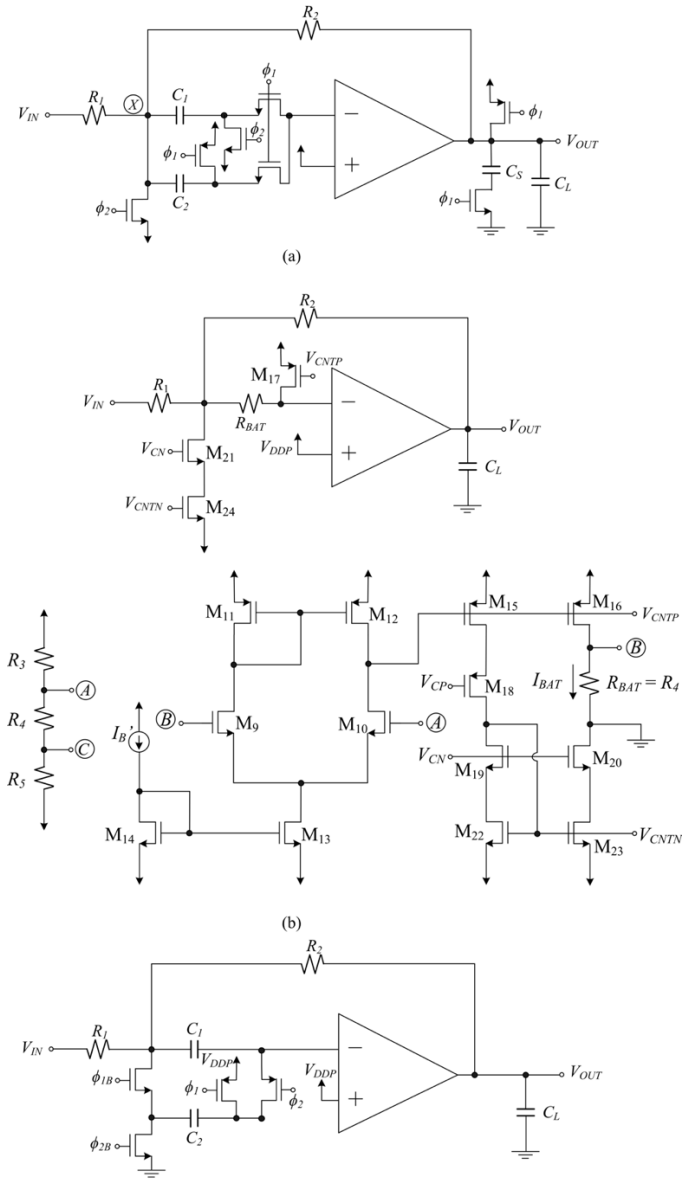

Figure 6.4. Low-Voltage Amplifiers (a) [2] (b) [3] (c) Proposed switched-capacitors approach

The three blocks that are going to be compared are displayed in Figure 6.4. Note that the circuit in Figure 6.4(b) is using the additional block in Figure 2.14 to create V_{CNTP} and V_{CNTN}. Switches have been implemented by transistors. PMOS transistors are employed when switches are connected to a voltage close to V_{DD}. In any other case, NMOS transistors are used. Clock signals are generated by a conventional scheme of non-overlapping clock generator, shown in Figure 6.5. Note the use of C_{gap} to increase the gap between the pulses. In the proposed topology, NMOS transistors implementing switches are controlled by boosted clocks, obtained from a clock doubler (which was depicted in Figure 3.11), to ensure they are totally open or close, since we are operating with voltages near their threshold voltage.

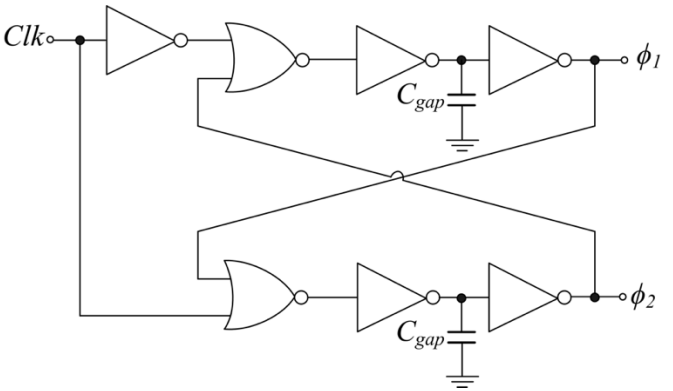

Figure 6.5. Non-overlapping clock generator block

Circuits in Figure 6.4 have been simulated with Cadence, using a 0.13 μm CMOS technology. Positive and negative supply voltages are ±0.3 V, bias current I_B is 10 μA and cascode voltages V_{CP} and V_{CN} are -50 mV and 50 mV, respectively. Transistor sizes are shown in Table 6.1. The value of resistors R_1 and R_2 that form the inverting stage is 100 kΩ, where resistors R_3, R_4 and R_5 has been set to 70 kΩ, 210 kΩ and 280 kΩ, respectively. Resistor R_{BAT} is 210 kΩ, as its value is the same as R_4. These values have been chosen in order to obtain V_{DDP} = 225 mV. Capacitors C_1 and C_2 have a value of 2 pF and load capacitors C_L are 20 pF.

Transistor	**W/L** (μm/nm)
M_1-M_2	10/210
M_3-M_4	30/210
M_5	60/210
M_6-M_8	20/210
M_9-M_{10}	10/210
M_{11}-M_{12}	30/210
M_{13}-M_{14}	20/210
M_{15}-M_{18}	60/210
M_{19}-M_{24}	20/210
M_{Rlarge}	0.3/160

Table 6.1. Transistors size of low voltage OTAs in Fig. 6.4

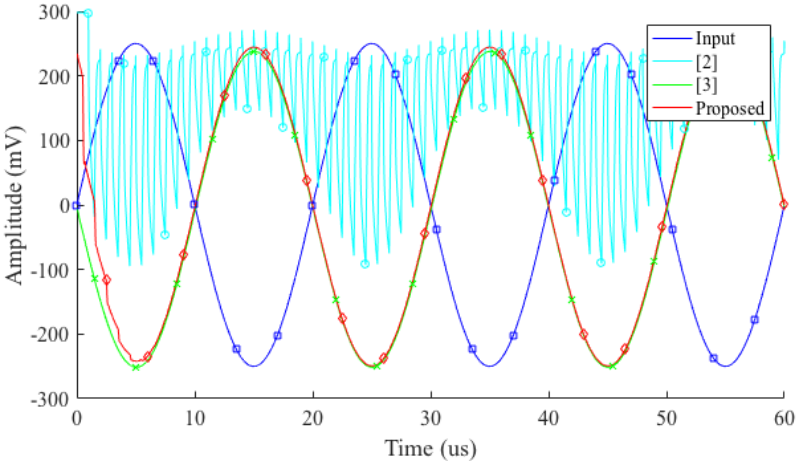

Figure 6.6. Simulated transient response of the three amplifiers

Figure 6.6 represents the transient response of the three amplifiers in Figure 6.4. Frequency of the clock signal is 1 MHz. As input voltage, a 0.6 V_{pp} 50 kHz sinusoidal signal has been used. As figure below shows, the output of Figure 6.4(a) should be V_{DD} in one phase and follow the input in the following phase. However, it requires high slew-rate, and circuit is slow when low supply voltage is used. Figure 6.4(b) and Figure 6.4(c) obtain the same output signal, verifying $V_{OUT} = -V_{IN}$. Nevertheless, the power consumption of the proposed circuit is lower than that of Figure 6.4(b), 12 μW vs 19.93 μW. Note that the

first cycles of the proposed circuit have some error, until *X* node reaches 0 V. After that, it works correctly.

Besides of simulated results, experimental measurements were obtained thanks to the prototype chip which was fabricated in the same 0.13 µm CMOS technology. It can be seen that the obtained results (shown in Figure 6.7) are similar to that obtained by simulation, except for the circuit of Figure 6.4(a), which works worse due to the higher experimental parasitic capacitance. In addition, the amplifier proposed in [3] does not reach the maximum amplitude. However, the proposed amplifier presents peaks caused by the switching between both phases.

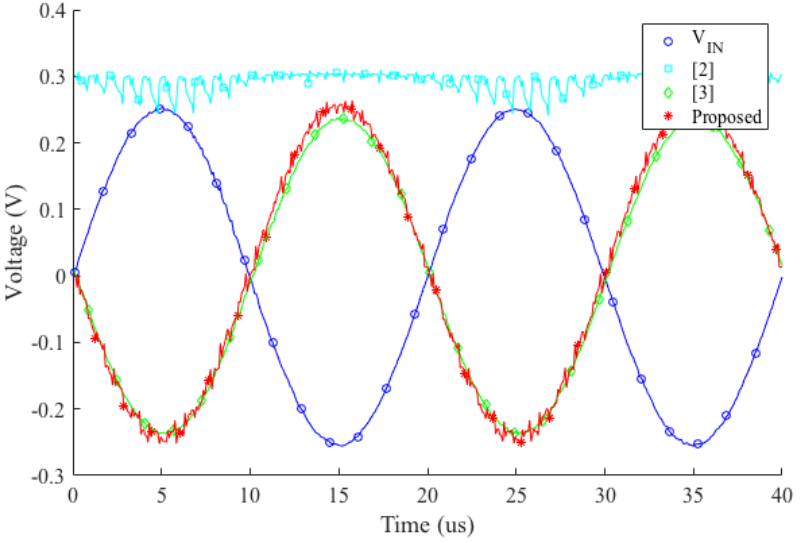

Figure 6.7. Measured transient response of the three amplifiers

Experimental THD measurements were also taken, obtaining -41.2 dB for the amplifier of Figure 6.4(b) and -45.3 dB for the proposed one, when a 0.5 V_{pp} 50 kHz sinusoidal signal was applied to the input.

Thus, thanks to switched capacitors an efficient amplifier is achieved, which is suitable for continuous-time applications.

6.2 Sample & Hold

The Sample and Hold (S&H) circuit is a fundamental block of an ADC circuit. It samples the input and holds this value for a certain time period. In its simplest form it consists of a sampling switch and a holding capacitor. A straightforward implementation of the switch is a transistor controlled by a clock through its gate voltage. This topology is presented in Figure 6.8 [4].

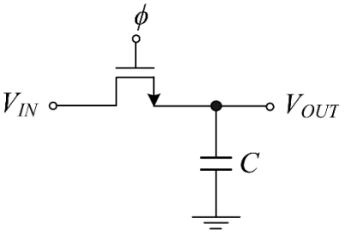

Figure 6.8. Simplest Sample and Hold

However, in practice S&H implementations often include amplifiers to improve accuracy. A conventional Sample and Hold circuit including an amplifier is shown in Figure 6.9 [4].

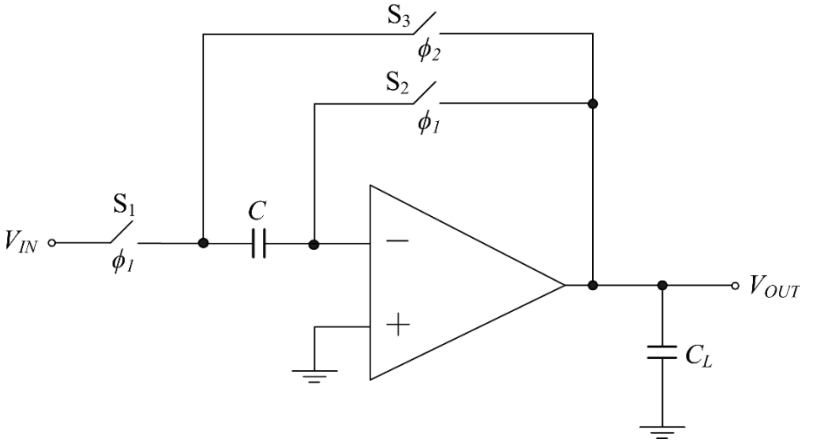

Figure 6.9. Conventional Sample and Hold

Conventional S&H circuits operate in two non-overlapping clock phases, ϕ_1 and ϕ_2. During ϕ_1, switches S_1 and S_2 are closed, whereas S_3 remains open. Thus, the input voltage is sampled in capacitor C and the output voltage

is 0 V. During phase ϕ_2, S_1 and S_2 open, while S_3 is closed, so the negative input terminal has a voltage of 0 V thanks to the amplifier's closed loop operation.

Fully differential topologies present some benefits over single-ended schemes, as it was said in Chapter 5. Starting from the conventional Sample and Hold circuit, the fully differential version can be constructed by duplicating the capacitor and switches $S_{1\text{-}3}$ in the positive input of the amplifier, and adding a CMFB circuit. The main advantage of a fully differential Sample and Hold circuit is that it does not require to reset the output to the input common-mode voltage, thus relaxing the slew rate requirements of the amplifier. However, this topology presents a limited input range. To avoid this problem, low voltage techniques can be applied in order to extend the input range, allowing rail-to-rail operation [5].

Figure 6.10 presents a proposed fully differential Sample and Hold. Low-voltage techniques explained in Chapter 2 have been employed. As shown in the figure below, besides the differential output terminals, the amplifier has two additional outputs, V_{OUTaux}+ and V_{OUTaux}-, whose purpose is to maintain a constant voltage V_{DDP} at the input. A CMFB circuit ensures this fact. This way, in phase ϕ_1, capacitors C store V_{id}-V_{DDP}, and in phase ϕ_2, the differential output voltage holds the value that V_{id} had at the end of phase ϕ_1. As the gate voltage of the differential pair is V_{DDP}, assuming NMOS amplifier input rail-to-rail operation is achieved.

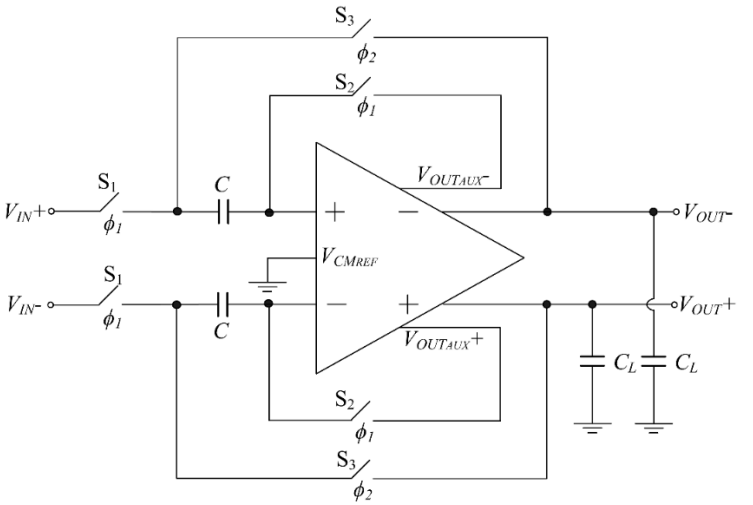

Figure 6.10. Proposed fully differential Sample and Hold

The employed amplifier is shown in Figure 6.11. It has two output stages, which are respectively used in each of the clock phases. In addition, the active load of the differential amplifier has been rearranged by using a LCMFB topology. The output stage that operates in phase ϕ_2 is class AB thanks to the QFG technique. As it can be seen from Figure 6.11, there are two CMFB circuits, one for the auxiliary output voltages, whose reference voltage is V_{DDP}, and the other one to adjust the output common-mode voltage to ground. Note that every switch has been implemented as NMOS transistors, controlled by non-overlapping boosted clocks (generated by circuits in Figure 3.11 and Figure 6.5). Table 6.2 indicates the component parameters in Figure 6.10 and Figure 6.11.

Component	Value	Component	Value
M_1-M_2	40 µm / 210nm	M_{Rlarge}	300 nm / 160 nm
M_3-M_4	75 µm / 210 nm	M_R	5 µm / 130 nm
M_5-M_8	150 µm / 210 nm	M_{SW}	500 nm / 130 nm
M_9-M_{10}	80 µm / 210 nm	R	50 kΩ
M_{11}-M_{14}	120 µm / 210 nm	R_{VDD}	15 kΩ
M_{15}-M_{16}	40 µm / 210 nm	R_{C1}	1 kΩ
M_{17}-M_{20}	75 µm / 210 nm	R_{C2}	5 kΩ
M_{21}-M_{22}	80 µm / 210 nm	C	1 pF
M_{23}-M_{24}	40 µm / 210 nm	C_{C1}	1 pF
M_{25}-M_{28}	75 µm / 210 nm	C_{C2}	4 pF

Table 6.2. Components' values of proposed S&H

Both the conventional S&H in Figure 6.9 (which employs the amplifier in Figure 6.3) and the proposed S&H have been simulated in a 0.13 µm CMOS technology. Supply voltages were set to ±0.3 V, and bias current I_B is 10 µA. Auxiliary voltage V_{DDP} is 200 mV. Two 20 pF grounded capacitors are employed as load.

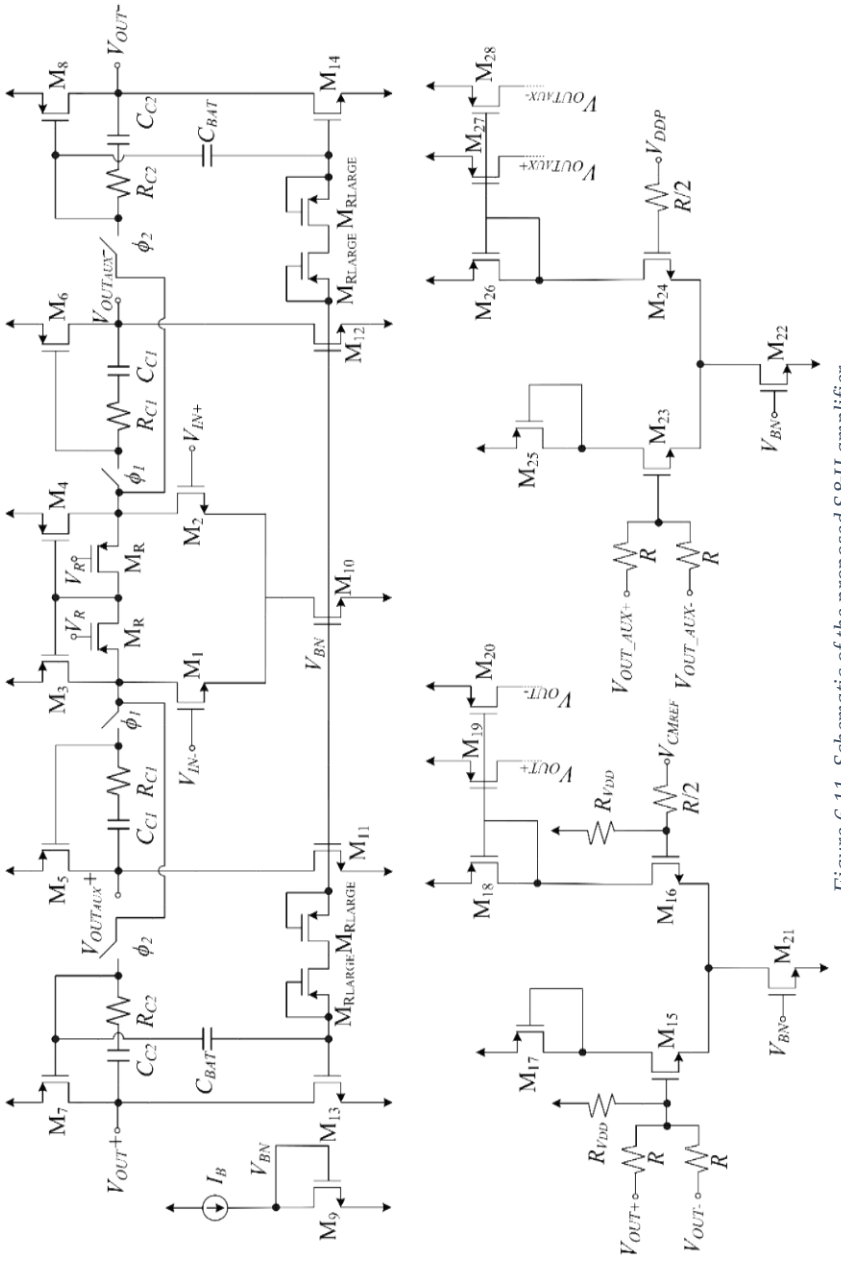

Figure 6.11. Schematic of the proposed S&H amplifier

The simulated transient response of both S&H circuits to a 50 kHz 0.5 V_{pp} sinusoidal input signal (also shown in the same picture) is included in Figure 6.12. The frequency of clocks is 1 MHz. Both S&H work properly but the fully differential S&H does not need to reset the output to V_{CMIN}, and it can operate rail-to-rail. Although its static power consumption is higher than the conventional topology, due to the inclusion of two CMFB circuits and two output branches, it consumes less power under dynamic conditions.

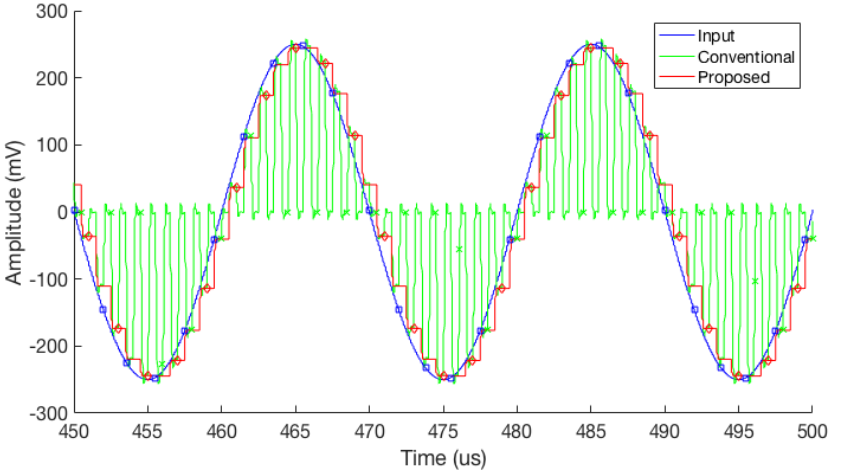

Figure 6.12. Input signal and corresponding conventional and proposed S&H transient response

Thus, an improved Sample and Hold fully differential circuit has been proposed. Thanks to its implementation, the input pair is biased so that it can process rail-to-rail input signals.

6.3 Delta Sigma modulator

Delta-Sigma modulators have been presented in Appendix D. In order to develop a Δ-Σ modulator, different blocks must be designed, which are displayed in Figure 6.13.

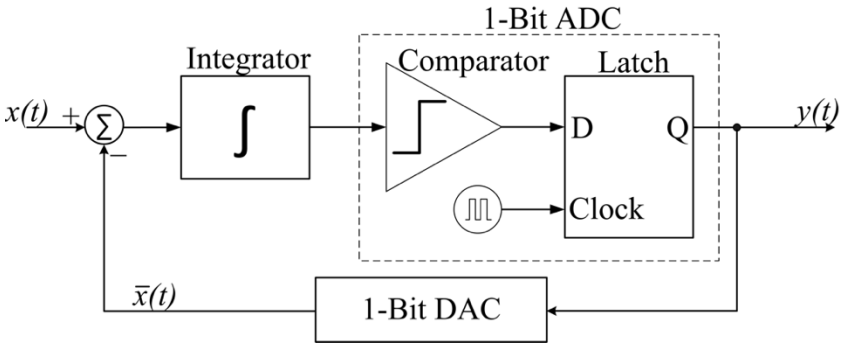

Figure 6.13. Conceptual scheme of a First-Order Delta-Sigma ADC

The first block that has been designed is the integrator. A conventional fully differential integrator is shown in Figure 6.14. It is formed by a fully differential amplifier, two resistors connected between the input terminals and the input of the amplifier for voltage-to-current conversion and two capacitors between the input and output terminals of the same amplifier to integrate the resulting currents.

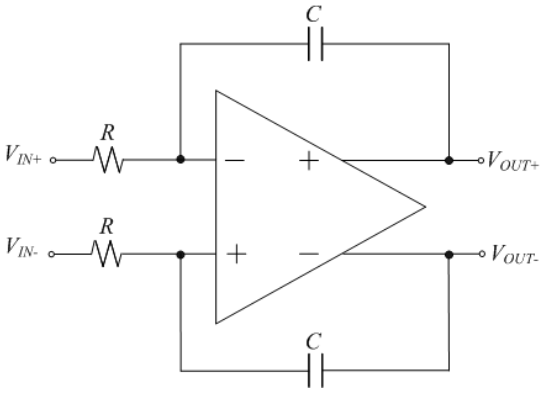

Figure 6.14. Conventional fully differential integrator topology

Switched capacitors are frequently used to implement the input resistors of the integrator. It is done by a capacitor and at least two switches that close in different phases, as Figure 6.15 indicates.

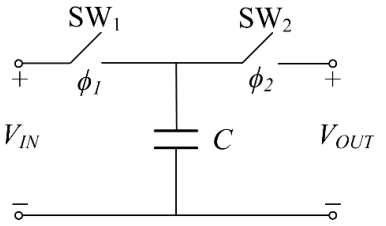

Figure 6.15. Basic Switched Capacitor Resistor

In phase ϕ_1, SW_1 is closed and SW_2 is open, hence capacitor C stores $q_{IN} = C \cdot V_{IN}$, whereas in phase ϕ_2, SW_1 is open and SW_2 is closed, so $q_{OUT} = C \cdot V_{OUT}$. Thus the charge moved out of the capacitor to the output is $q = q_{IN} - q_{OUT} = C \cdot (V_{IN} - V_{OUT})$. The definition of current is the amount of charge transferred per unit time, i.e. $I = q \cdot f$, being f the switching frequency. Substituting the expression of q, we obtain $I = C \cdot (V_{IN} - V_{OUT}) \cdot f$. Considering V the voltage across the SC from the input to the output ($V = V_{IN} - V_{OUT}$), the equivalent resistance R is:

$$R = \frac{V}{I} = \frac{1}{C \cdot f} \tag{6.1}$$

Based on this idea, Figure 6.16 shows a fully differential integrator that employs switched capacitors as resistors. Besides, by connecting the capacitor to the output of the 1-bit DAC shown in Figure 6.13, the subtraction between the input $x(t)$ and its prediction $\bar{x}(t)$ is obtained.

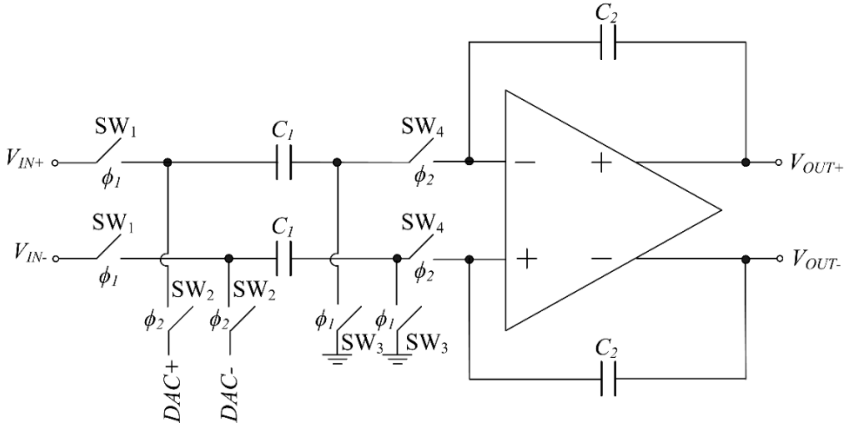

Figure 6.16. Fully differential integrator with switched-capacitor resistors

However, this topology is not suitable for low-voltage applications, as it has a limited input range. In order to achieve rail-to-rail operation, switched-capacitors are modified so that the input pair of the amplifier is biased by a higher voltage V_{DDP}, based on the same idea that was explained in Chapter 2 and that is used in the previous S&H. The proposed low-voltage integrator is displayed in Figure 6.17.

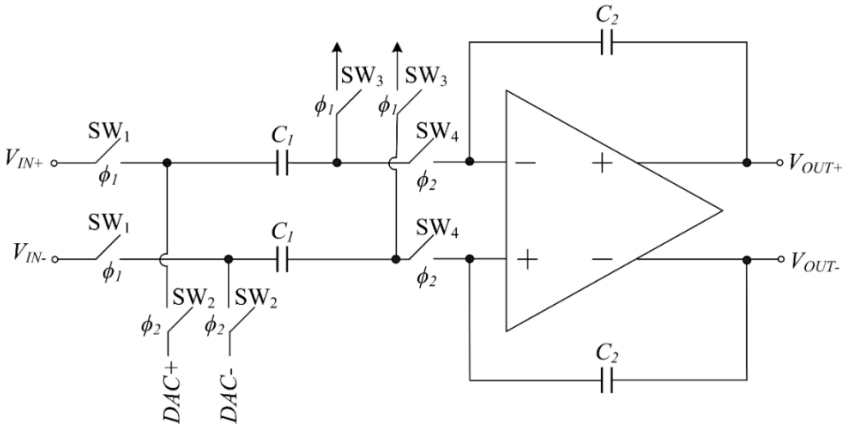

Figure 6.17. Low voltage integrator

In both cases, the same amplifier has been used, which is shown in Figure 6.18(a). It is a two-stage OTA, which uses an adaptive LCMFB scheme at the active load of the first stage (explained in Chapter 4) and a QFG class AB output stage. Note that for the conventional topology, the CMFB circuit employed is that on Figure 6.18(b), and for the proposed low voltage version, the CMFB is that on Figure 6.18(c).

As the prediction error $x(t)$- $\bar{x}(t)$ is quite small, so as the signal obtained by the integrator, a common practice is the use of a preamplifier before the quantizer, thus obtaining higher resolution. Figure 6.19 shows its scheme.

In phase ϕ_1, the input of the first amplifier is connected to ground, so only its offset (V_{OS1}) is amplified, this is $A_1 \cdot V_{OS1}$, being A_1 the gain of the first amplifier. As the switches of the second amplifier are also closed, it is connected in unity gain configuration, thus its differential output voltage is its offset V_{OS2}. Since capacitors C_3 are connected between the outputs of both amplifiers, these capacitors store $V_C = V_{OS2} - A_1 \cdot V_{OS1}$. However, in phase ϕ_2, the differential input signal is connected to the first amplifier, obtaining at its output $A_1 \cdot (V_{IN} + V_{OS1})$. Since C_3 were previously charged to V_C, the offset of the first stage is

compensated. The second amplifier scales its input, which is $(A_1 \cdot V_{IN} + V_{OS2}) - V_{OS2} = A_1 \cdot V_{IN}$, thus compensating the offset of the second amplifier. This way, the obtained output voltage is $A_1 \cdot A_2 \cdot V_{IN}$.

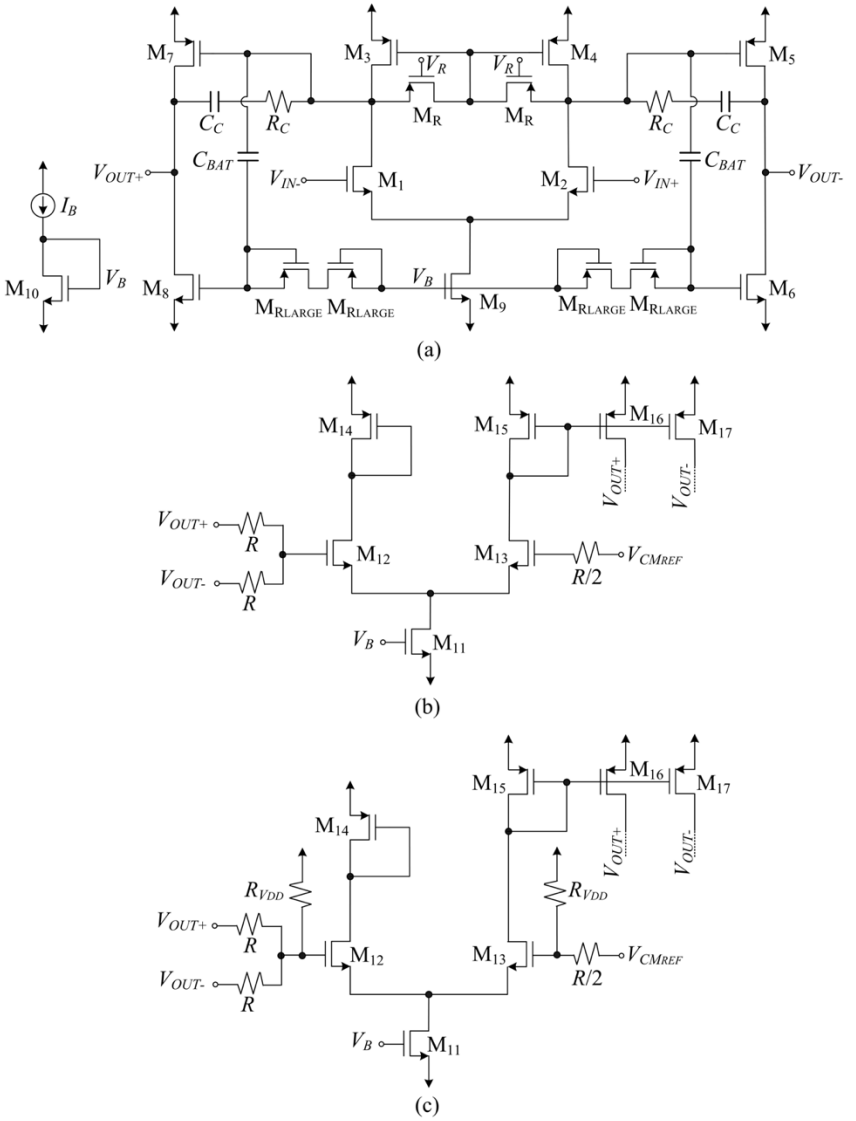

Figure 6.18. Amplifier of the integrator (a) OTA employed in both conventional and LV (b) CMFB circuit of conventional integrator (c) CMFB circuit of LV integrator

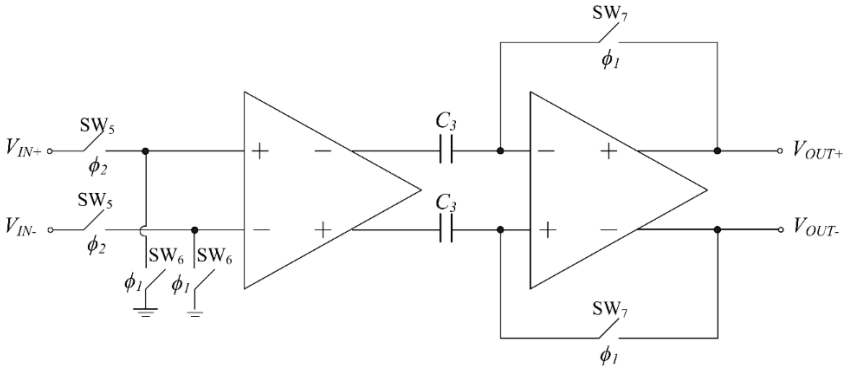

Figure 6.19. Preamplifier of the Delta-Sigma converter

Single-stage differential pairs with LCFMB active load have been employed as amplifiers, which are shown in Figure 6.20. Since the amplitude of input differential signal is small, there is no need to modify the topology to achieve rail-to-rail operation, thus the same schematic works for both conventional and low supply voltage versions.

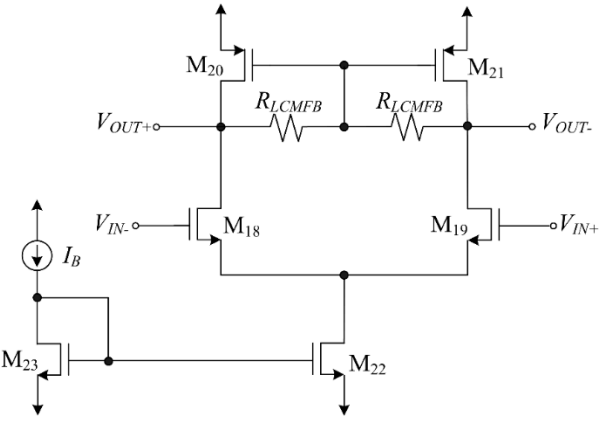

Figure 6.20. Single stage amplifier used in pre-amplifier block

After the preamplifier, a track and latch stage is employed as comparator. Its schematic is displayed in Figure 6.21. When $V_{IN+} > V_{IN-}$, transistors M_{24} and M_{26} are off, whereas M_{25} and M_{27} are on. In ϕ_1 switches SW_8 are closed, the voltage at node *B* is V_{DD}, and that of node *A* is V_{SS}. However, in ϕ_2, the voltage at these nodes becomes V_{SS} due to switches SW_9. Thus, voltage at node *A* is V_{SS} but node *B* experiences swings between V_{DD} (in ϕ_1) and V_{SS} (in ϕ_2). Switches SW_{10} are closed a bit later than SW_9, making voltage at node *C* to

maintain a constant voltage V_{DD} in both phases while node *D* toggles between V_{SS} (in ϕ_1) and V_{DD} (in ϕ_2), just the opposite of node *B*. Finally, as SW_{11} close at next ϕ_1 (a bit delayed), the inverted output is V_{SS} for both phases, and V_{OUT} is V_{DD}. When $V_{IN+} < V_{IN-}$, nodes *A* and *B* exchange their behavior, as well as nodes *C* and *D*. Note that when there is a transition at the output of the comparator, it happens one cycle after input signals have changed. Delayed clocks have been used to connect the inverters to ensure their proper operation. In addition, this topology is also suitable for low supply voltages, as transistors are acting as switches.

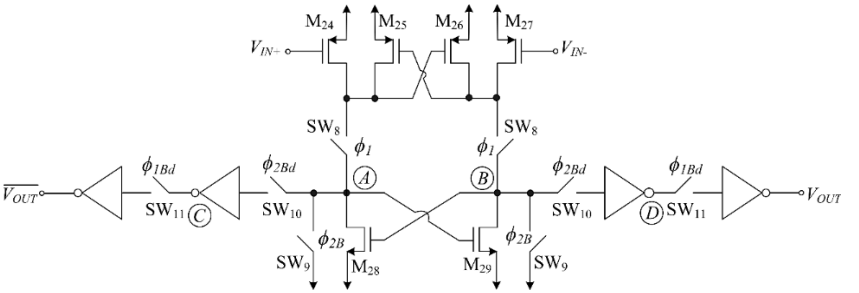

Figure 6.21. Track and Latch comparator

The last block to design is the 1-bit DAC. Although the output of the Sigma Delta modulator is already a digital signal, its amplitude has to be reconditioned in order to be comparable with that of the input signal. Figure 6.22(a) indicates the conceptual scheme of the DAC. Its output must be V_{REF+} or V_{REF-}, depending on a control signal, which in this case is the output of the Delta-Sigma modulator. The implementation of the DAC is shown in Figure 6.22(b), employing transistors as switches.

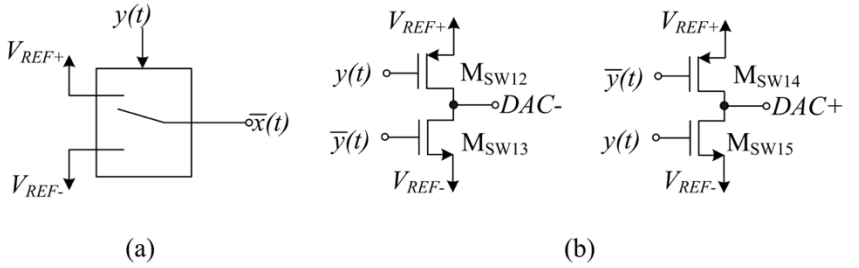

Figure 6.22. 1-bit Digital-to-Analog converter

Two Delta-Sigma modulators are built with the previously presented blocks: the first one will be supplied by two ±0.6 V complementary voltage

sources, and the second one is the low-voltage version of the former, whose supply voltages are half of the conventional, i.e. ±0.3 V. Bias current I_B is 10 μA. Table 6.3 indicates the values of different devices employed. The inverter block has been implemented in conventional configuration, whose PMOS and NMOS transistors have aspect radios of 60 μm/210 nm and 30 μm/210 nm, respectively. Reference voltages V_{CMREF} of Figure 6.18(b) and Figure 6.18(c) are both connected to ground, as the modified LCFMB circuit shifts the voltage at gates of differential pair thanks to R_{VDD}. The reference voltages V_{REF+} and V_{REF-} of the conventional Sigma Delta modulator are ±0.45 V and that of the proposed one are ±225 mV, respectively.

Component	Value	Component	Value
M_1-M_2	40 μm / 210nm	M_{SW8}	60 μm / 210 nm
M_3-M_4	75 μm / 210 nm	M_{SW9}	20 μm / 210 nm
M_5, M_7	150 μm / 210 nm	$M_{SW10\text{-}11}$	500nm / 130 nm
M_6, M_8	120 μm / 210 nm	$M_{SW12\text{-}15}$	1.5 μm / 160 nm
M_9-M_{11}	80 μm / 210 nm	M_{Rlarge}	300 nm / 160 nm
M_{12}-M_{13}	40 μm / 210 nm	M_R	5 μm / 130 nm
M_{14}-M_{17}	75 μm / 210 nm	R	50 kΩ
M_{18}-M_{19}	40 μm / 210 nm	R_{VDD}	15 kΩ
M_{20}-M_{21}	75 μm / 210 nm	R_C	5 kΩ
M_{22}-M_{23}	80 μm / 210 nm	R_{LCMFB}	40 kΩ
M_{24}-M_{27}	60 μm / 210 nm	C_C	4 pF
M_{28}-M_{29}	20 μm / 210 nm	C_1	1 pF
$M_{SW1\text{-}4}$	500nm / 130 nm	C_2	3.5 pF
$M_{SW5\text{-}7}$	1.5 μm / 160 nm	C_3	2 pF

Table 6.3. Parameter values of Sigma-Delta modulator

Figure 6.23 and Figure 6.24 show the response of both Delta-Sigma modulators to a 50 kHz 450 mV_{pp} and 225 mV_{pp} sinusoidal signal, respectively. These signals should be demodulated in order to obtain $\bar{x}(t)$. However, this process requires a lot of samples (leading to a huge computational load).

Thus, an improved Sigma Delta has been obtained by applying a low voltage low power technique, which was explained in Section 2.2.1. Thanks to this, the supply voltage was reduced to half of that of the conventional block.

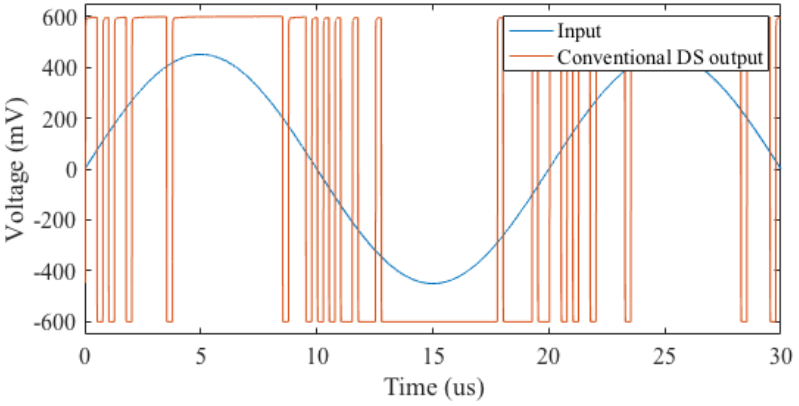

Figure 6.23. Conventional Delta-Sigma response

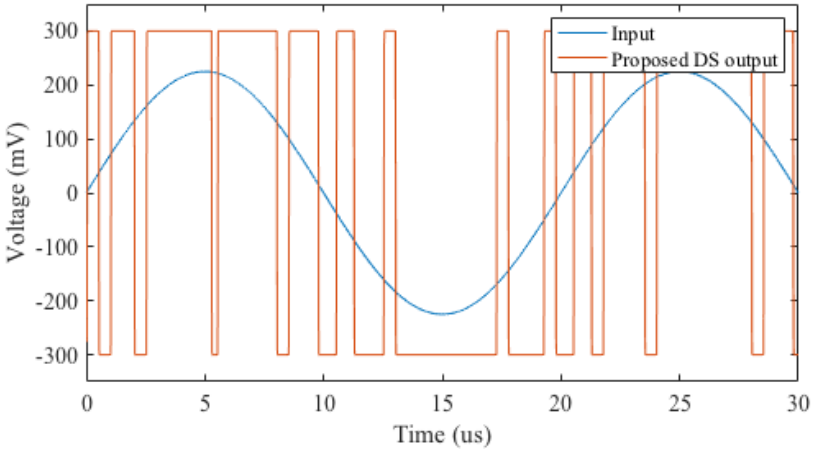

Figure 6.24. Proposed Low-Voltage Delta-Sigma response

6.4 Conclusions

In this Chapter, three low voltage subsystem blocks have been introduced. First block is a low power buffer, which is based on switched capacitors. The second and third blocks are related to A/D conversion: a Sample and Hold and a Sigma Delta modulator. The three proposed circuits are capable of operating in low voltage conditions, making them suitable for energy harvesting supplied systems.

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Chapter 7

CONCLUSIONS AND FUTURE WORK

In this Chapter, the most significant results and conclusions reported throughout this thesis are summarized. The objective of Section 7.1 is to provide a compilation of the main contributions to verify the fulfillment of the objectives proposed in Chapter 1. In addition, future research directions related to this work are proposed and briefly analyzed in Section 7.2.

7.1 Conclusions

Almost all the work done in this Ph. D. thesis has been based on the application of low voltage low power techniques to analog design, and more specifically to amplifiers, in order to obtain different blocks suitable for systems with strict energy constraints, such as those employing energy harvesting. The motivation is the growing demand of portable devices supplied by batteries in IoT scenarios, which require to extend the lifetime of the battery or even to get rid of such battery in some cases. In the following paragraphs, general conclusions are provided following the structure of this document, i.e. first the proposed new cells are addressed to end with the design of complete subsystems.

Chapter 2 has presented the state of the art of low voltage low power methodologies, in order to achieve class AB amplifiers with high current efficiency and rail-to-rail operation. Note that these techniques can be applied

at device level (in this case, at transistor level) or at circuit level. Special attention has been paid to Quasi-Floating Gate (QFG) transistors, the adaptive biasing of the input pair (especially that formed by two cross-coupled floating batteries) and the Local Common Mode Feedback (LCMFB) configuration.

In Chapter 3, the conventional CMOS logic gate family has been revisited and adapted to subthreshold operation by using QFGMOS transistors. Besides, two applications of these logic gates have been presented: a ring oscillator and a clock doubler. Thanks to QFGMOS transistors, the voltage supply requirements have been relaxed, and faster subthreshold logic gates have been obtained.

Several single-ended amplifiers have been proposed in Chapter 4, which is formed by three subsections, depending on the topology these amplifiers are based on: telescopic cascode amplifier, folded cascode amplifier and recycling folded cascode. All the proposed amplifiers presented higher transconductance (thus GBW), higher SR values, lower input referred noise density (mainly caused by the higher G_m) and nearly ideal current efficiency (CE). It is worth mentioning the particular case of a RFC combining an adaptive bias scheme at the input stage and a Local Common-Mode Feedback topology at the folding stage, which achieved an increase factor on the SR of 66 vs. the conventional folded cascode amplifier. In Section 4.2, not only the proposed OTAs have been compared, but also other opamps previously published by other authors. In order to ease that comparison, two Figure of Merits have been employed, evidencing the improvements of the proposed blocks.

Chapter 5 contains different blocks related to fully differential amplifiers. First, an improved Common-Mode Feedback (CMFB) circuit has been proposed, which has been used to control the output common-mode voltage of a super class AB OTA. After that, several class AB fully differential OTAs have been proposed, all of them with improved transconductance (thus A_{DC} and GBW) and SR. As happened in Chapter 4, a final Section has been included, addressing a comparison of the proposed OTAs and other ones previously published by other authors, in which the former ones presented higher values of Figures of Merit.

Finally, subsystem level blocks have been presented in Chapter 6, two of them related with Analog to Digital converters (ADCs): a Sample and Hold and a Delta Sigma modulator. Apart from that, a low voltage buffer has been proposed, which despite using switched capacitors, it is suitable for continuous

time applications. In the three cases, although their supply voltages have been decreased, they enhance their respective conventional versions.

7.2 Future Work

Although different proposals have been made throughout this thesis at device, circuit and subsystem level, much work is still to be made. Some new possible directions are specified below.

- For some of the blocks, only simulation results have been provided, as they have not been fabricated. Thus, these blocks can be fabricated in order to validate their advantages by measurements.

- Most of the prototype chips have been fabricated in a 0.5μm CMOS technology, which is very reliable but also old-fashioned and with large threshold voltages. More modern technologies can be employed to obtain faster designs able to operate at lower supply voltages.

- The majority of the proposed amplifiers have been designed following single-ended topologies. In Chapter 5, the advantages of fully differential implementations have been enumerated, such as higher input range and lower THD. Thus, the proposed amplifiers can be redesigned with differential output in order to improve their features even more.

- Several amplifiers have been proposed at cell level, obtaining improved performance when compared with conventional topologies. These amplifiers can be employed at system level to take advantage of its characteristics.

- In Chapter 6, a low voltage Sigma Delta Modulator was presented. However, only simulated time response graphs have been included. Thus, a more in-depth analysis must be performed.

Appendix A

SETUP DESCRIPTION

In this Appendix, the experimental setup employed for the different measurements carried out is going to be explained. However, before addressing the different setups, some extra circuitry will be described. When fully differential OTAs are measured, two additional blocks may be needed depending on the test equipment available: a voltage subtractor and a differential signal generator.

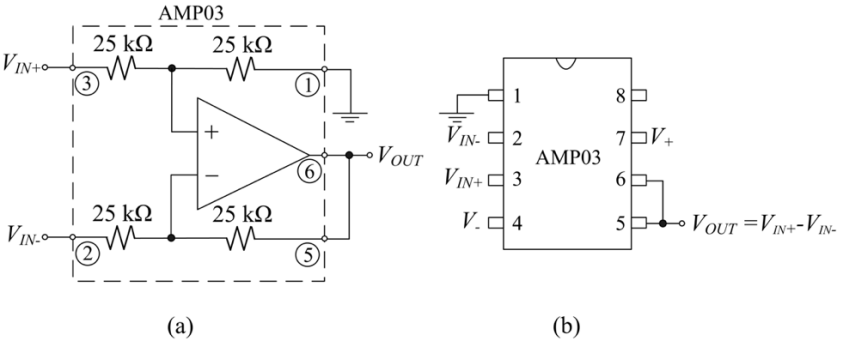

Figure A.1. Subtractor circuit (a) Schematic (b) Implementation

A well-known structure of a subtractor is shown in Figure A.1(a). The resulting output voltage is $V_{OUT} = V_{IN+} - V_{IN-}$. Thanks to the use of an AMP03 Precision Unity-Gain Differential Amplifier from Analog Devices, an easy implementation is obtained, as depicted in Figure A.1(b). Voltages V_+ and V_-

represent the positive and negative supply voltages, respectively. These voltages are defined in the datasheet of the AMP03, which are typically ±15 V.

The second block is a differential signal generator. For AC measurements, $V_{IN+} = V_{CM} + V_{id}/2$ and $V_{IN-} = V_{CM} - V_{id}/2$ are required. However, in practice, a vector signal analyzer is employed for AC input generation, which provides a chirp signal in one of its ports. This signal must be converted from single-ended to differential form. For that purpose, circuit in Figure A.2 is used. The obtained output signals are

$$V_{IN+} = V_{CM} + \frac{R_2}{R_1} V_{id} \tag{A.1}$$

$$V_{IN-} = V_{CM} - \frac{R_2}{R_1} V_{id} \tag{A.2}$$

As in the AMP03, $R_1 = R_2 = 25$ kΩ, factor $R_2/R_1 = 1$. Thus, the amplitude of the differential input voltage V_{id} should be half to compensate this effect.

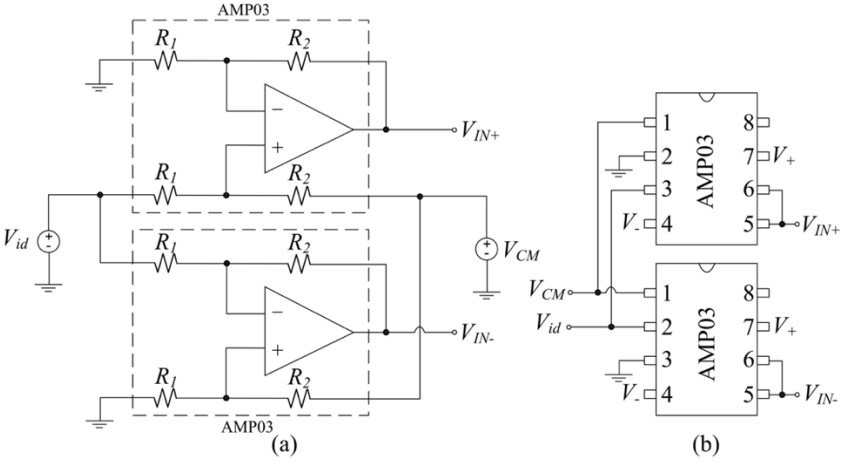

Figure A.2. Differential signal generator (a) Schematic (b) Implementation

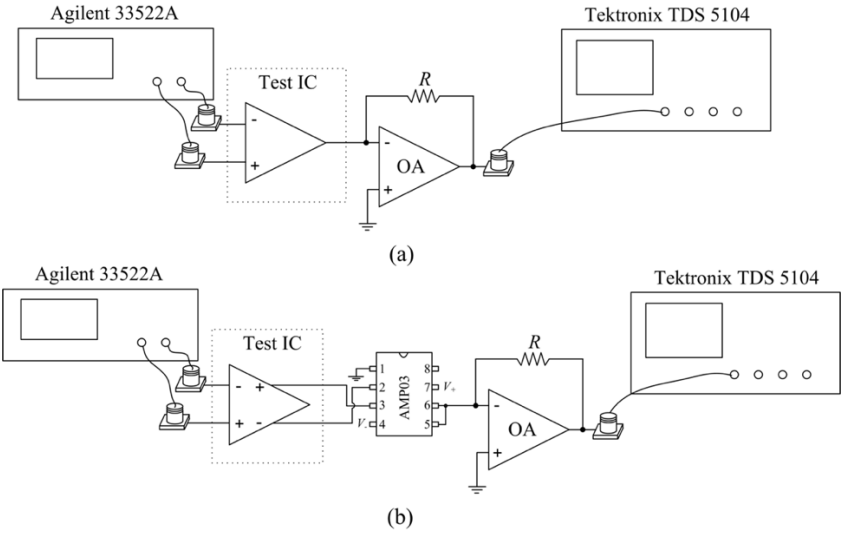

Figure A.3. Output current measurements setup (a) Single-ended (b) Fully-differential

The setup employed for output current measurements is depicted in Figure A.3. The OTAs in open loop configuration are driven by the differential output of an Agilent 33522A arbitrary waveform generator, and the output of the device under test is connected to a transresistance amplifier for voltage-to-current conversion. The resulting voltage is applied to a Textronix TDS 5104 oscilloscope for capture and display. In the case of fully differential topologies, a subtractor circuit is placed between the target OTA and the transresistence amplifier, as shown in Figure A.3(b).

As shown in Figure A.4, for time-domain measurements the Agilent 33522A signal is applied to the OTAs in unity-gain closed-loop configuration and the unbuffered output is directly connected to the TDS 5104 oscilloscope using a conventional test probe. For distortion analysis the output signal is applied to a Hewlett Packard 89410A Vector Signal Analyzer. Note that when the topology of the amplifier is fully differential, the unity-gain close-loop configuration requires four matched R resistors, which are always fabricated on-chip.

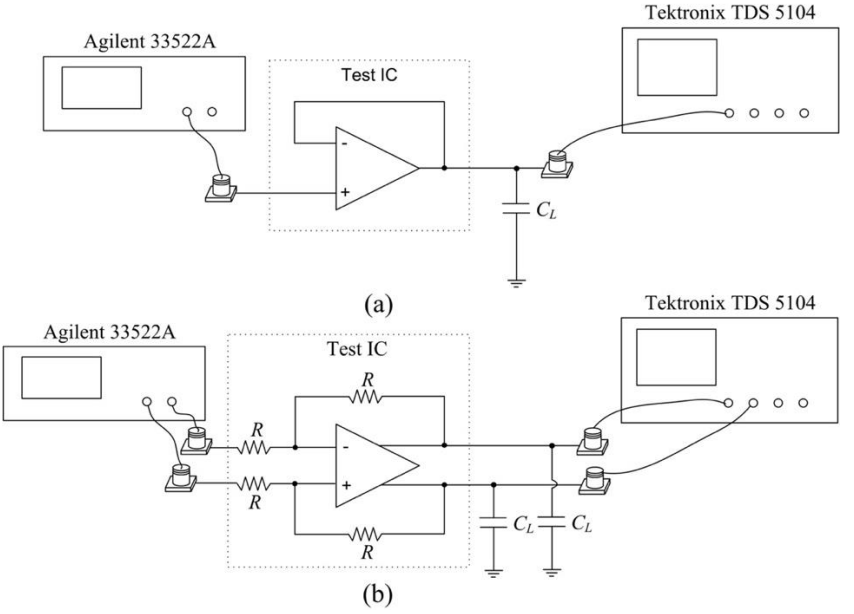

Figure A.4. Transient response measurement setup (a) Single-ended (b) Fully Differential

The HP 89410A is also used for frequency response measurements as shown in the figure below, using a chirp sweep. Since the amplifier is measured in unity-gain closed-loop configuration, its cutoff frequency corresponds to the GBW assuming a single dominant pole behavior. For fully differential amplifiers, the previously described differential signal generator is needed to provide valid input signals. The Agilent 33522A is employed to set the common-mode input voltage so that the DC operating point of the transistors is well defined. In addition, the differential output signal is converted to single-ended form by the subtractor block.

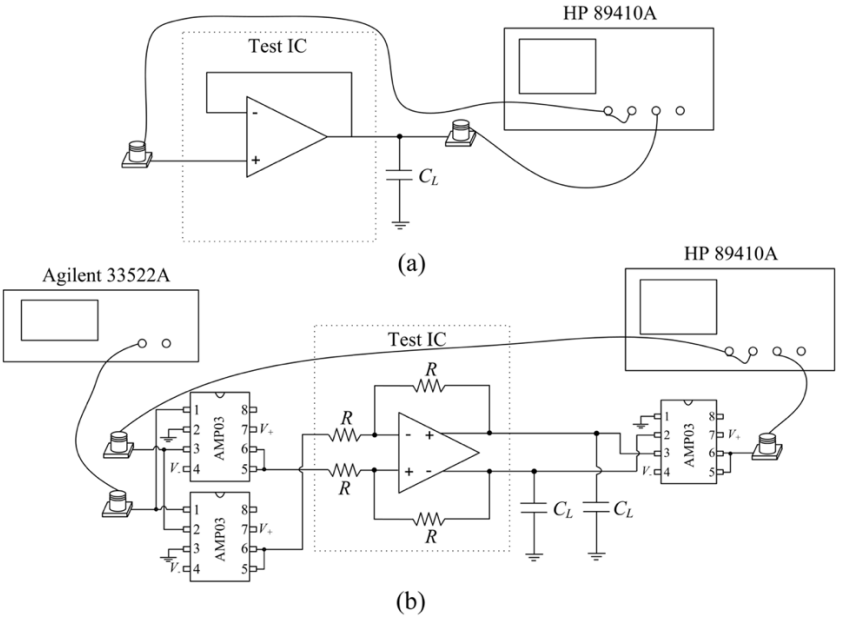

Figure A.5. Frequency response measurements setup (a) Single-ended (b) Fully differential

The setup employed for noise measurements is shown in Figure A.6. An external amplifier with gain A is used to amplify noise, and its output is connected to the HP 89410A. In order to obtain the equivalent input noise, two steps must be done. First, the noise density of the setup without the chip is measured, and then the noise density of the whole setup is measured again. This way, the equivalent input noise voltage density of the amplifier is calculated following the expression

$$V_{nIC}^2 = \frac{1}{A}\sqrt{V_{nALL}^2 - V_{nAMPs}^2} \tag{A.3}$$

being V_{nALL}^2 the noise voltage density of the whole setup (see Figure A.6) and V_{nAMPs}^2 the noise voltage density of the auxiliary amplifiers (substractor and external amplifier with gain *A*). Note that for both single-ended and fully differential topologies, the Agilent 33522A is employed to set the DC operating point of the amplifier.

It is worth mentioning that normally, the equivalent input noise in a certain bandwidth *Δf* is given. To obtain this value, the noise density must be

integrated in Δf. Since the flicker noise is not considered (due to the relatively high bandwidth of the tested devices) and the thermal noise is constant, the input-referred noise is calculated as the product of the noise density and the squared root of Δf.

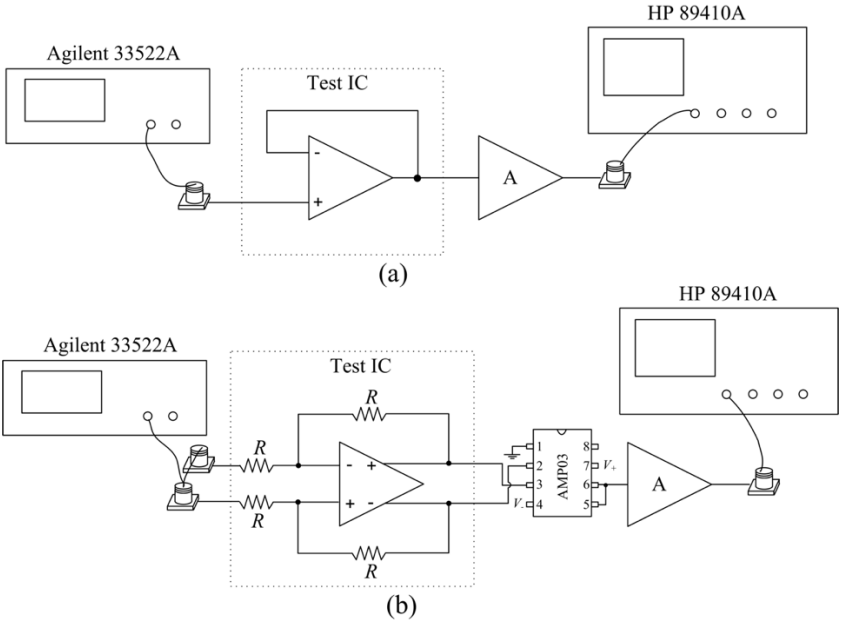

Figure A.6. Noise measurements setup (a) Single-ended (b) Fully differential

Appendix B

NOISE ANALYSIS OF THE IMPROVED RFC

The most relevant noise sources in CMOS analog circuits are thermal and flicker noise. Assuming operation in saturation, a simplified expression of the mean square value of the noise current of a MOS transistor is [1]

$$I_n^2(f) = 4\delta k_B T g_m + \frac{K_f g_m^2}{WLC_{oxf}} = 4\delta k_B T g_m + \frac{2\mu K_f I_D}{L^2 f} \quad \text{(B.1)}$$

with k_B the Boltzmann's constant, T the absolute temperature, μ the carrier mobility and K_f a technology-dependent parameter which is also dependent on device characteristics. Factor δ varies from 1/2 to 2/3 from weak to strong inversion. The first and second terms in Equation B.1 correspond to the thermal and flicker noise, respectively. The expression B.1 represents a good trade-off between simplicity, accuracy and validity in all the inversion regions.

Assuming as usually that all noise sources are uncorrelated, and for simplicity the same δ factor for all transistors, the input-referred thermal noise of the FC OTA is

$$\overline{v_{nt,inFC}^2} = \frac{2\delta k_B T \Delta f}{g_{m1A}}\left(2 + \frac{g_{m3A}}{g_{m1A}} + \frac{g_{m3B}}{g_{m1A}} + \frac{g_{m9}}{g_{m1A}}\right) \quad \text{(B.2)}$$

and that of the RFC OTA is

$$\overline{v_{nt,inRFC}^2} = \frac{8\delta k_B T \Delta f}{g_{m1A}(1+K)^2}\left(1 + K^2 + (1+K)\frac{g_{m3A}}{g_{m1A}} + \frac{g_{m9}}{g_{m1A}}\right) \tag{B.3}$$

which for the implemented value of K=3 becomes

$$\overline{v_{nt,inRFC}^2} = \frac{2\delta k_B T \Delta f}{g_{m1A}}\left(\frac{5}{2} + \frac{g_{m3A}}{g_{m1A}} + \frac{1}{4}\frac{g_{m9}}{g_{m1A}}\right) \tag{B.4}$$

The expression for the super class AB RFC OTA is

$$\overline{v_{nt,inAB}^2} = \frac{2\delta k_B T \Delta f}{g_{m1A}}\left[\begin{array}{c}\frac{g_{m3A}+g_{m9}}{g_{m1A}(1+g_{m3A}R)^2} + \frac{1+2(g_{m3A}R)^2}{(1+g_{m3A}R)^2} \\ + \frac{1}{g_{m1A}}\left(\frac{g_{m3A}R}{1+g_{m3A}R}\right)^2\left(g_{m3B} + \frac{1}{\delta R}\right)\end{array}\right] \tag{B.5}$$

which for R>>$1/g_{m3A}$ becomes

$$\overline{v_{nt,inAB}^2} = \frac{2\delta k_B T \Delta f}{g_{m1A}}\left[2 + \frac{g_{m3A}}{g_{m1A}} + \frac{1}{\delta g_{m1A} R}\right] \tag{B.6}$$

Concerning flicker noise, assuming again uncorrelated noise sources and the same K_f for all the transistors of the same type (NMOS or PMOS) the resulting expression for the FC OTA is:

$$V_{nf,inFC}^2(f) = \frac{2K_{fp}}{C_{ox}fW_1L_1}\left[1 + \left(\frac{L_1}{L_9}\right)^2 + 2\frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\left(\frac{L_1}{L_3}\right)^2\right] \tag{B.7}$$

and for the RFC OTA it is

$$V_{nf,inRFC}^2(f) = \frac{2K_{fp}}{C_{ox}fW_{1A}L_{1A}}\left[\begin{array}{c}\frac{1+K^2}{(1+K)^2} + \frac{2}{(1+K)^2}\left(\frac{L_{1A}}{L_9}\right)^2 \\ + \frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\frac{K}{1+K}\left(\frac{L_{1A}}{L_{3B}}\right)^2\end{array}\right] \tag{B.8}$$

The input-referred flicker noise of the super class AB RFC OTA is

$$V_{nf,inAB}^2(f) = \frac{K_{fp}}{2C_{ox}fW_{1A}L_{1A}(1+g_{m3A}R)^2}\left\{\begin{array}{c}1 + 2\left(\frac{L_{1A}}{L_9}\right)^2 + 3\frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\left(\frac{L_{1A}}{L_{3B}}\right)^2 + \\ +(g_{m3A}R)^2\left[2 + \frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\left(\frac{L_{1A}}{L_{3B}}\right)^2\right]\end{array}\right\} \tag{B.9}$$

In this design, all the transistors were implemented with the same L (the minimum one available in the technology), so that expressions for the flicker noise of the FC OTA, RFC OTA with K=3 and super class AB RFC OTA with R>>$1/g_{m3A}$ are

$$V_{nf,inFC}^2(f) = \frac{4K_{fp}}{C_{ox}fW_1L_1}\left(1 + \frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\right) \quad \text{(B.10)}$$

$$V_{nf,inRFC}^2(f) = \frac{4K_{fp}}{C_{ox}fW_{1A}L_{1A}}\frac{3}{8}\left(1 + \frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\right) \quad \text{(B.11)}$$

$$V_{nf,inAB}^2(f) = \frac{4K_{fp}}{C_{ox}fW_{1A}L_{1A}}\frac{3}{8}\left(\frac{2}{3} + \frac{1}{3}\frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\right) \quad \text{(B.12)}$$

Bibliography

[1] D. A. Johns and K. Martin, “Analog integrated circuit design”, *John Wiley & Sons*, 1997.

Appendix C

SLEW RATE ANALYSIS OF THE IMPROVED RFC

The theoretical SR for the super class-AB RFC OTA of Figure 4.17 will be derived for simplicity using the conventional square-law drain current model for transistors in the saturation region, and neglecting channel length modulation and short- channel effects. Thus, if a large positive V_{id} is applied, current in transistor M_{2B} becomes

$$I_{2B} = \frac{\beta_{2B}}{2}\left(\sqrt{\frac{I_B}{\beta_{2B}}} + V_{id}\right)^2 \tag{C.1}$$

with $\beta_{2B}=\mu_p C_{ox}(W/L)_{2B}$. Current in transistors M_{1A} and M_{1B} becomes negligible. Hence a differential current $I_d=I_{2A}-I_{1B} \approx I_{2A}$ flows in the differential pair M_{1B}-M_{2B}, yielding a current $I_d/2$ flowing through the resistors. Current in transistors M_{3B}, M_{3C}, M_{4B} and M_{4C} is $I_{cm}= (I_{2A}+I_{1B})/2\approx I_{2A}/2$. Therefore, current in transistor M_{3A} becomes

$$I_{3A} = \frac{\beta_{3A}}{2}\left(\sqrt{\frac{2I_{cm}}{\beta_{3B}}} + \frac{R_1 I_d}{2}\right)^2 \approx \frac{\beta_{3A}}{2}\left(\sqrt{\frac{I_{2A}}{\beta_{3B}}} + \frac{R_1 I_{2A}}{2}\right)^2 \tag{C.2}$$

while current in M_{4A} becomes negligible due to the large negative swing at its gate created by the voltage drop at R_2. This rises the drain voltage of M_{4A} and

drives M_{2A} into deep triode. The large current I_{3A} is mirrored by the PMOS current mirror M_9-M_{10}, yielding an output current

$$I_{out} \approx \frac{\beta_{3A}}{2}\left(\sqrt{\frac{2I_{cm}}{\beta_{3B}}} + \frac{R_1 I_d}{2}\right)^2 \approx \frac{\beta_{3A}}{2}\left(\sqrt{\frac{\beta_{2B}}{2\beta_{3B}}} V_{id} + \frac{R_1\beta_{2B}}{4} V_{id}^2\right)^2 \quad \text{(C.3)}$$

Hence, for a differential input step of A volts, the SR_+ is resulted in Equation 4.23. Similarly, for a large negative $-V_{id}$ it can be found that the output current is

$$I_{out} \approx -\frac{\beta_{4A}}{2}\left(\sqrt{\frac{\beta_{1B}}{2\beta_{4B}}} V_{id} + \frac{R_2\beta_{1B}}{4} V_{id}^2\right)^2 \quad \text{(C.4)}$$

where the minus sign denotes current entering the OTA. Thus, for a differential input step A, Expression 4.24 is obtained.

Appendix D

INTRODUCTION TO A/D CONVERSION

Nowadays, analog and digital signals have to coexist, as both are used to transmit information by transforming it into electric signals. The difference between analog and digital technologies is that in analog technology, information is translated into electric signals of varying amplitude, whereas in digital domain, translation of information is into binary format, represented by two different amplitude levels.

Conversion between the analog and digital domain is a common process in communication systems, either from digital to analog domain, such as the reproduction of an mp3 audio file though a speaker, or from analog to digital, e.g. a sound picked up by a microphone or light entering a digital camera.

As its name indicates, Analog-to-Digital converters (ADC) convert analog information into a digital signal, making these discrete data suitable for digital systems [1]. As Figure D.1 displays [1], the conversion implies three steps: sampling, quantization and coding.

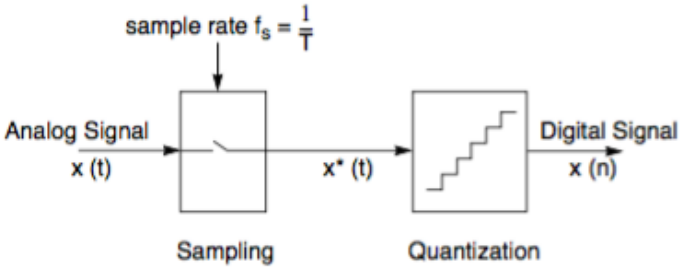

Figure D.1. Analog to Digital Conversion Process

Analog signals are characterized by being continuous in amplitude (and usually also in time) and it is necessary to convert them to a sequence of numbers that are only defined at determined (or discrete) instants of time, which are proportional to the sampling period T_S [1]. A discrete-time signal $x^*(t)$ can be represented by a sampled continuous-time signal $x(t)$ as:

$$x^*(t) = \sum_{n=-\infty}^{\infty} x(t)\delta(t - nT) \qquad \text{(D.1)}$$

where $\delta(t)$ is known as Dirac's delta, and is defined as $\delta(t) = 1$ only for $t = 0$, and 0 in any other case.

Most ADCs can be divided into two groups: Nyquist rate converters and oversampling converters. In the former ones, the maximum frequency of the analog signal is slightly less than the Nyquist frequency, $f_N = f_S/2$, where f_S is the sampling frequency, whereas the latter ones perform the sampling process at a much higher rate, $f_N << f_S$.

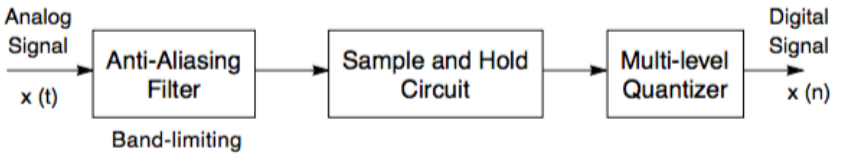

Figure D.2. Conventional Analog to Digital Conversion Process

A very common practice, as shown in Figure D.2, is to use an anti-aliasing filter before sampling the signal. The anti-aliasing filter consists on a low-pass filter whose response is flat over the frequency band of interest and attenuates the frequencies above the Nyquist frequency. This way, signal distortion due to aliasing is avoided. Figure D.3(a) and Figure D.3(b) show aliasing distortion and the effects of the anti-aliasing filter, respectively [1].

After an anti-aliasing filter, a Sample and Hold circuit is employed (Figure D.2). The purpose of this block is to maintain its output constant

between samples so that the signal can be quantized properly. If the output of the sample and hold varies during T_S, it can limit the performance of the ADC converter subsystem.

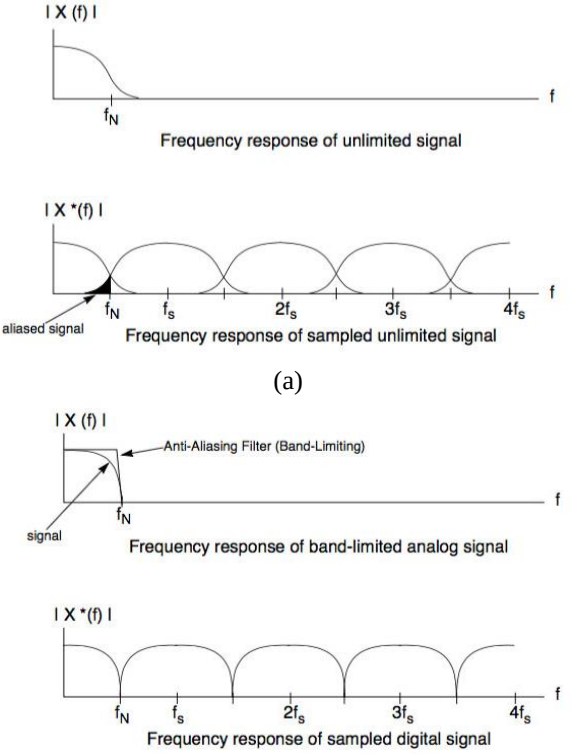

Figure D.3. Aliasing distortion and result of using an anti-aliasing filter

The final block of a conventional ADC is the quantizer. It compares the sampled analog signal to a set of reference levels, which are assigned to a digital code. Depending on the result of the comparison, a digital encoder generates the code corresponding to the level the input signal is closest to. The number of quantization levels is dependent on the number of bits of resolution, $N = 2^B$, being N the number of voltage intervals and B the number of bits used by the encoder. One of the most relevant parameters of an ADC is the resolution, which is the minimum change in voltage required to guarantee a change in the output code level. The voltage resolution is the overall voltage measurement range divided by the number of intervals: $Q = E_{FSR}/N$, with E_{FSR} the full scale voltage range or span, given by the difference between the upper and lower voltages that

can be coded: $E_{FSR} = V_{RefHi} - V_{RefLow}$. This Q value is also known as Less Significant Bit, or LSB. The greater the number of bits *N*, the smaller the error of quantization, improving the accuracy [3].

Hence, the relationship between the sampled discrete signal *x(n)*, the sampled continuous signal $x^*(t)$ and the quantization noise or quantization error is:

$$x(n) = x^*(t) + e(n) \tag{D.2}$$

When the input signal is low (comparable to LSB), the quantization error is dependent on the input signal, resulting in distortion, known as dither. This distortion is created after the anti-aliasing filter, and if they are above half the sample rate, they will alias back into the band of interest. In order to make quantization error independent of the input signal, noise with an amplitude of $2 \cdot Q$ is often added to the signal, reducing signal to noise ratio (SNR), but ideally, completely eliminating the distortion.

However, in the typical case where the original signal is much larger than one LSB, the quantization error is not significantly correlated with the signal, and has an approximately uniform distribution. Its value depends on the quantization method: in the rounding case, the quantization error has a mean of zero and the RMS value is the standard deviation of this distribution, given by $\sigma_e = \left(1/\sqrt{12}\right) \cdot Q \approx 0.289 \cdot Q$, whereas in the truncation case, the mean is $\mu_e = (1/2) \cdot Q$ and the RMS value is $\sigma_e = \left(1/\sqrt{3}\right) \cdot Q$. From the standard deviation, quantization noise power, or variance is directly obtained as σ_e^2.

Since the noise power σ_e^2 is spread over the entire frequency range equally, noise power spectral density can be expressed as $N(f) = \sigma_e^2 / f_s$. If the input signal is larger than the LSB step, the noise power spectral density is defined in Equation D.3. In addition, Figure D.4 shows the noise spectrum of Nyquist samplers.

$$N(f) = \frac{Q^2}{12 f_s} \tag{D.3}$$

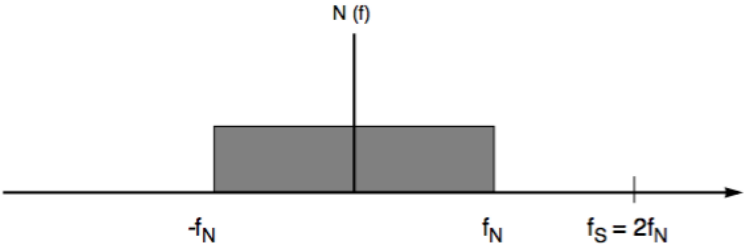

Figure D.4. Noise PDF of Nyquist samplers

On the other hand, oversampling converters present some benefits versus Nyquist samplers. One of them concerns the anti-aliasing filter. Nyquist-rate converters require a low pass filter with stringent requirements, as its pass-band response must be flat with not phase distortion (linear phase), and for frequencies above its cutoff frequency, the frequency response must decay abruptly, which in practice is difficult to achieve. Nevertheless, if the sampling rate is $N \cdot f_S$, the requirements of the anti-aliasing filter are relaxed, as the transition band of the filter can be much wider.

Besides, oversampling has beneficial effects on noise power, because the total noise power for both samplers is the same (defined in Equation D.3), but the percentage of this noise that is in the bandwidth of interest in oversampling converters is smaller, which is defined by Equation D.4. The bigger F_S compared to f_B, the smaller the noise. This concept is depicted in Figure D.5.

$$N_B = \int_{-f_B}^{f_B} N(f)df = \frac{Q^2}{12}\frac{2f_B}{F_S} \quad \text{(D.4)}$$

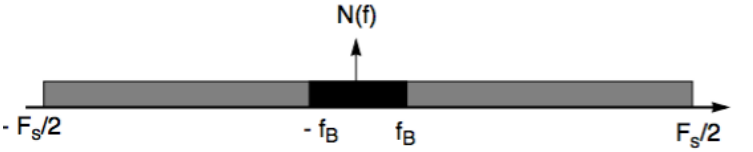

Figure D.5. Noise Spectrum of Oversampling A/D Converters

Delta-Sigma modulation is one of the most effective forms of conversion in the data converter world. Its applications include communication systems, professional audio and precision measurements. But for a better understanding, here is a brief explanation about how delta modulation works. Figure D.6 includes delta modulation and demodulation schemes and their corresponding signals. A higher transmission efficiency is achieved by

quantifying only the changes (delta) in value between consecutive samples, rather than the actual samples themselves, assuming that contiguous samples are highly correlated.

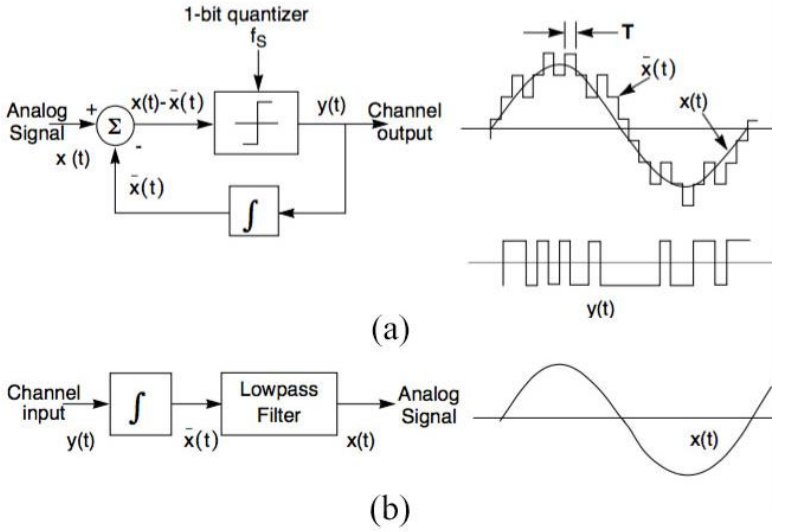

Figure D.6. Delta modulation (a) Modulator (b) Demodulator

The integrator of the feedback loop works as a predictor, as the output of the integrator tries to predict input. The difference between the input *x(t)* and the predicted signals $\bar{x}$(t) (also known as prediction error) is quantized and used to make the next prediction. In order to recover the analog input signal, the receiver must accumulate the bits and low pass filter that signal.

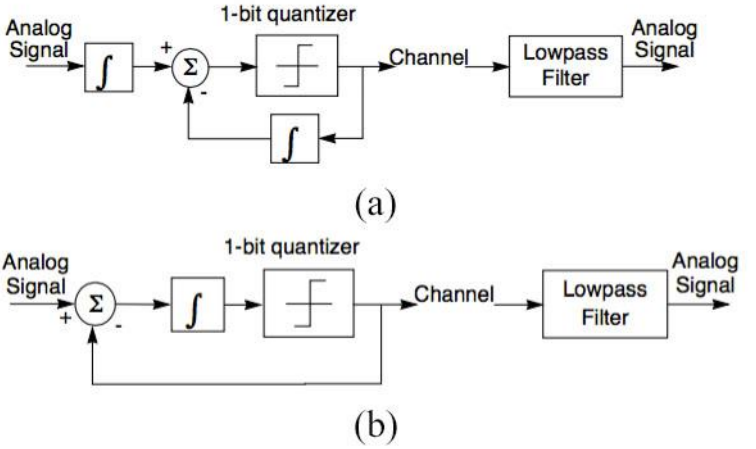

Figure D.7. Delta-Sigma Modulation (a) Two-integrators (b) Only one integrator

However, delta modulation requires two integrators for modulation and demodulation. Since integration is a linear operation, the second integrator can be moved before the modulator without altering the overall characteristics. In addition, the two integrators can be combined into a single integrator by the linear operation property. Figure D.7 shows this transformation. Scheme in Figure D.7(b) is known as Delta-Sigma modulator, or Δ-Σ.

Sigma-Delta converters present a very advantageous feature. They perform a quantization noise-shaping, resulting in an improved output signal. This property is very useful in signal processing applications. When the Δ-Σ modulator is analyzed in *s*-domain (see Figure D.8), the integrator becomes 1/*s*.

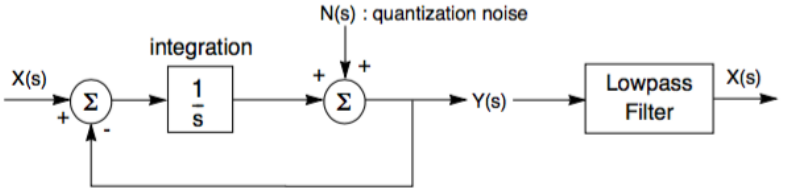

Figure D.8. S-Domain analysis of Sigma-Delta Modulator

If signal transfer function is calculated, a low-pass filter response is observed, while as for the noise transfer function, a high-pass filter is obtained. Equations D.5 and D.6 express signal and noise transfer functions respectively.

Hence, the input signal does not change as long as its frequency is not higher than the low-pass filter cutoff frequency and the noise is pushed to higher frequencies, so most of it is rejected by the low-pas filter.

$$Y(s) = [X(s) - Y(s)]\frac{1}{s} \rightarrow \frac{Y(s)}{X(s)} = \frac{\frac{1}{s}}{1+\frac{1}{s}} = \frac{1}{s+1} \quad \text{(D.5)}$$

$$Y(s) = -Y(s)\frac{1}{s} + N(s) \rightarrow \frac{Y(s)}{N(s)} = \frac{1}{1+\frac{1}{s}} = \frac{s}{s+1} \quad \text{(D.6)}$$

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APPENDIX D: INTRODUCTION TO A/D CONVERSION

LIST OF PUBLICATIONS

International Journals

1. J. M. Algueta-Miguel, A. Lopez-Martin, M. P. Garde, C. A. De la Cruz and J. Ramirez-Angulo, "±0.5 V 15 μW recycling folded cascode amplifier with 34767 MHz·pF/mA FOM", *IEEE Solid-State Circuits Letters*, Jan. 2019.

2. M. P. Garde. A. Lopez-Martin, R. G. Carvajal, J. A. Galan and J. Ramirez-Angulo, "Super class AB RFC OTA using nonlinear current mirrors", *Electronics Letters*, vol. 54, no. 23, pp. 1317-1318, Nov. 2018.

3. M. P. Garde. A. J. Lopez-Martin, R. G. Carvajal and J. Ramirez-Angulo, "Super class AB RFC OTA with adaptive local common-mode feedback", *Electronics Letters*, vol. 54, no. 22, pp. 1272-1274, Nov. 2018.

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5. A. Lopez-Martin, M. P. Garde, J. M. Algueta, C. A. De la Cruz-Blas, R. G. Carvajal and J. Ramirez-Angulo, "Enhanced single-stage folded cascode OTA suitable for large capacitive loads", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 4, pp. 441-445, Apr. 2018.

6. M. P. Garde, A. Lopez-Martin and J. Ramirez-Angulo, “Power-efficient class AB telescopic cascode opamp”, *Electronics Letters*, vol. 51, no. 10, pp- 620-622, May 2018.

7. J. M. Saso, A. Lopez-Martin, M. P. Garde and J. Ramirez-Angulo, “Power-efficient single-stage class AB fully differential amplifier”, *Electronics Letters*, vol. 53, no. 19, pp. 1298-1300, Sep. 2017.

8. A. Lopez-Martin, M. P. Garde and J. Ramirez-Angulo, “Class AB differential difference amplifier for enhanced common-mode feedback”, *Electronics Letters*, vol. 53, no. 7, pp. 454-456, Mar. 2017.

International Conferences

1. M. P. Garde, A. Lopez-Martin, R. G. Carvajal and J. Ramirez-Angulo, “Micropower single-stage amplifier based on adaptive biasing and class AB current follower”, *XXXIII Conference on Design of Circuits and Integrated Systems (DCIS 2018)*, Lyon, France, 2018.

2. M. Pilar Garde, A. López-Martín, D. Orradre and J. Ramirez-Angulo, “Ultra-low power subthreshold quasi floating gate CMOS logic family for energy harvesting”, *28th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, Platja d’Aro, Spain, 2018.

3. M. P. Garde, A. Lopez-Martin, R. G. Carvajal and J. Ramirez-Angulo, “Folded cascode OTA with 5540 MHz·pF/mA FoM”, *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018.

4. A. Lopez-Martin, M. P. Garde, R. G. Carvajal and J. Ramirez-Angulo, "On the optimal current followers for wide-swing current-efficient amplifiers", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018.

5. J. M. Algueta, A. Lopez-Martin, C. A. De la Cruz Blas, M. P. Garde, J. R. Garcia-Oya, J. Garcia-Doblado, F. Muñoz-Chavero, V. Baena-Lecuyer and E. Hidalgo-Fort, "Ultrasonic communication through metallic walls for monitoring applications", *32nd Conference on Design of Circuits and Integrated Systems (DCIS)*, Barcelona, Spain, 2017.

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7. C. A. De La Cruz-Blas, M. P. Garde and A. Lopez-Martin, "Super class AB transconductor with slew-rate enhancement using QFG", *2017 European Conference on Circuit Theory and Design (ECCTD)*, Catania, Italy, 2017.

8. M. P. Garde, A. Lopez-Martin and J. Ramirez-Angulo, "Enhanced differential super class AB OTA", *13th Conference on PhD Research in Microelectronics and Electronics (PRIME)*, Taormina, Italy, 2017.

9. M. P. Garde, A. Lopez-Martin and J. Ramirez-Angulo, "Improved common-mode feedback based on LCMFB techniques", *13th Conference on PhD Research in Microelectronics and Electronics (PRIME)*, Taormina, Italy, 2017.

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12. A. Lopez-Martin, D. Orradre, M. P. Garde, P. Sanchis, E. Gubia, G. Perez, D. Astrain and J. Ramirez-Angulo, “Energy-harvesting microsystems based on the QFG MOS transistors”, *15th International Conference on Environment and Electrical Engineering (EEEIC)*, Rome, Italy, 2015.

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